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Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, January 1 to December 31, 1976

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D. L. Blackburn, R. Y. Koyama,
F. F. Oettinger, and G. J. Rogers

Electronic Technology Division
Institute for Applied Technology
National Bureau of Standards
Washington, D.C. 20234

March 1977

Issued May 1977

Prepared for
Energy Research and Development Administration
Division of Electric Energy Systems
Washington, D.C. 20545

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PREFACE

This work was conducted as a part of the Semiconductor Technology Program in the Electronic Technology Division of the National Bureau of Standards (NBS). This program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. Its major thrusts are the development of carefully evaluated and well documented test procedures and associated technology and the dissemination of such information to the electronics community. Application of the output by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. The output provides a common basis for the purchase specifications of government agencies which will lead to greater economy in government procurement. In addition, improved measurement technology will provide a basis for controlled improvements in fabrication processes and in essential device characteristics.

The segment of the Semiconductor Technology Program described in this annual report is supported by the Division of Electric Energy Systems in the Office of Conservation at the Energy Research and Development Administration (ERDA) under ERDA Contract No. E(49-1)-3800 Modification No. 3. The contract is monitored by Dr. A. S. Clorfeine of ERDA. The NBS point of contact for information on the various task elements of this project is F. F. Oettinger of the Electronic Technology Division at the National Bureau of Standards. The work reported herein also drew upon the results of studies carried out under the part of the Semiconductor Technology Program funded by the Defense Advanced Research Projects Agency under Order No. 2397, Program Code 6D10.

Certain commercial equipment, instruments, or materials are identified in this report in order to adequately specify the experimental procedure. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

Measurement Techniques for High Power Semiconductor Materials and Devices

ANNUAL REPORT
January 1 to December 31, 1976

By

D. L. Blackburn, R. Y. Koyama,
F. F. Oettinger, and G. J. Rogers

EXECUTIVE SUMMARY

This annual report describes NBS activities directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from rapidly increasing demands for electricity and the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for thyristors and rectifier diodes. Application of this measurement technology will, for example, enable industry to make devices with higher individual power handling capabilities, thus permitting very large reductions in the cost of power handling equipment and fostering the development of direct current (dc) transmission lines to reduce energy waste and required rights-of-way.

The major tasks under this project are (1) to evaluate the feasibility of the photovoltaic method as a rapid, nondestructive technique for characterizing the resistivity uniformity of high-resistivity, large-diameter silicon wafers and (2) to evaluate the use of thermally stimulated current and capacitance measurements as a means for characterizing lifetime controlling or leakage source defects in power device grade silicon wafers.

Photovoltaic Technique — One of the principal characteristics specified in the procurement of silicon for high power devices is the radial variation of resistivity which results from an inhomogeneous doping density. When fabricating high power devices, both the solid-state diffusion and alloying steps are affected by the presence of variations in the doping density. Because of this, poor junction geometry and nonuniform current distributions are frequent problems in devices fabricated from inhomogeneous material. Device failures due to hot spots or thermal runaway may result. Gross variations in resistivity also cause wide variations in device characteristics and contribute to poor device yields. As an example, a localized low resistivity region of a wafer limits operating voltages of a

device fabricated from that wafer to values lower than those expected from the remainder of the wafer.

In the photovoltaic technique, a light spot is scanned along a wafer diameter. The photovoltage and photo-induced change in specimen resistance are measured as a function of position along the wafer diameter. From these two measurements, the variation in resistivity along the diameter can be computed. The technique requires no contact upon the wafer surface area where a finished device or devices are to be fabricated. Thus, unlike the presently used methods for determining the resistivity gradients of silicon wafers, this technique is non-destructive.

During this reporting period, the design and construction of a prototype automated measuring system capable of displaying the resistivity profile along two perpendicular diameters of large-diameter, high-resistivity silicon wafers were nearly completed. Considerable effort was expended on attempts to develop improved methods for making electrical contact to the wafer. Two systems have been developed for this purpose, one employing a knife-edge contacting scheme at the wafer rim, the other employing a point probe contacting scheme on the wafer surface near the rim. As of this reporting period, neither contacting system was fully operational.

Work is now underway to evaluate the performance of the two contacting schemes and to determine the effects of design changes made to the basic measurement system.

Thermally Stimulated Measurements — Thermally stimulated current and capacitance measurements (TSM) utilize the ability of defects to emit majority carriers in the depletion region of semiconductors after receiving sufficient thermal energy. Defects are charged at low temperature (78 K) and the test structure is heated at a high rate to cause emission of the charge. The emitted charge is measured as a current in the external circuit; this emission also results in a slight collapse of the depletion region causing an increase in the depletion capacitance. The behavior of the emission with heating rate and temperature is unique to a particular defect. Suitable analysis of the measured data can yield the energy level, emission rate, and the density of the defect. The utility of TSM to power device grade silicon is evident. It would allow characterization and identification of defects which control the switching properties and the leakage of high power thyristors.

During this reporting period, a procedure was developed for the utilization of thermally stimulated measurements to evaluate starting material for power device use. This in-

volved the low temperature fabrication of MOS capacitors as the test vehicle for TSM; the low temperature is necessary to avoid alteration or introduction of defects into the starting material by the fabrication procedure.

Typically high power devices are fabricated on individual silicon wafers ranging in diameter from 10 to 80 mm. This necessitated the development of TSM apparatus to handle wafer-sized specimens. A thermally controllable chuck was developed to handle wafers as large as 65 mm. It has a temperature range covering 78 K to 625 K with heating rates as high as 7 K/s. The wafer chuck was adapted to a modified wafer prober, and the entire apparatus was housed in a hermetic enclosure for ambient control.

Details of power device processing were investigated by visits to a number of major thyristor manufacturing facilities. These studies revealed that TSM could be utilized at intermediate steps in the normal processing of typical thyristors, provided that appropriate test structures could be fabricated. The low temperature MOS fabrication procedure was suited for starting material evaluation. Several possible procedures are being developed for the fabrication of test structures on the diffused power device wafer. The general goal is to fabricate mesa diodes utilizing the existing junction in the wafer.

Measurement procedures are being investigated to establish standard techniques for the TSM analysis of defects and to document interferences which could distort or confuse the desired TSM response. Although specific analysis of defects in power grade material awaits the routine fabrication of mesa diodes, several interferences have been observed.

1. INTRODUCTION

This project is directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from rapidly increasing demands for electricity and the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for thyristors and rectifier diodes.

The project is designed to provide, disseminate, and foster the standardization of improved measurement methods required in high power semiconductor technology, for use in specifying materials and devices in commerce, and, by industry, in controlling device manufacturing processes and in designing systems. Application of this measurement technology will, for example, enable industry to: (1) make power semiconductor de-

vices with greater uniformity of characteristics, thus permitting improvements in parallel and series connections of devices for applications from fusion generation to ac/dc conversion, (2) make devices with higher individual power handling capabilities, thus permitting very large reductions in the cost of power handling equipment and fostering the development of direct current (dc) transmission lines to reduce energy waste and required rights-of-way, and (3) provide devices, and the systems utilizing them, with the reliability and performance required in energy generation, utilization, and conservation.

The major tasks under this project are (1) to evaluate the feasibility of the photovoltaic method as a rapid, nondestructive technique for characterizing the resistivity uniformity of high resistivity, large-diameter silicon wafers and (2) to evaluate the use of thermally stimulated current and capacitance measurements as a means for characterizing lifetime controlling or leakage source defects in power device grade silicon wafers.

2. PHOTOVOLTAIC TECHNIQUE

2.1 Objectives

The overall objective of this task is to evaluate the feasibility of the photovoltaic method [1,2] as a rapid, nondestructive technique for characterizing the resistivity uniformity of high-resistivity, large-diameter silicon wafers. In the photovoltaic technique, a light spot is scanned along a wafer diameter. The photovoltage and photo-induced charge in specimen resistance are measured as a function of position along the wafer diameter. From these two measurements, the variation in resistivity along the diameter can be computed. Phase 1 of the task, January 1, 1976 to October 1, 1976, had the following objectives:

1.1 Develop a suitable system for making contact to the edge of the circular silicon wafer; a key to this objective is the development of a system that provides good mechanical alignment of the contacts and a means for making improved nonrectifying contacts to the wafer edge.

1.2 Design and construct a prototype automated measuring system capable of displaying or printing out the resistivity profile along two perpendicular diameters of large-diameter, high-resistivity silicon wafers.

Phase 2 of the task, October 1, 1976 to October 1, 1977, has the following objectives:

2.1 Characterize the automated photovoltaic system for measuring resistivity uniformity of high-resistivity, large-diameter silicon wafers; this objective involves a determination of the spa-

tial resolution, applicable resistivity range, and feasibility of simplifying the measurement procedure.

2.2 Document the automated photovoltaic system for measuring resistivity uniformity of high-resistivity, large-diameter silicon wafers; this objective involves the writing of a manual detailing the operation and construction of the system.

To date, efforts have been undertaken in all areas except in objective 2.2. Efforts are now being concentrated in Phase 2 of this task which is scheduled for completion in FY-77. This section of the report will discuss the progress that has been made toward each of these objectives.

2.2 Background

a. Importance of Resistivity and Resistivity Variation for Power Devices

One of the principal characteristics specified in the procurement of silicon for high power devices is the radial variation of resistivity which results from an inhomogeneous doping density. When fabricating high power devices, both the solid-state diffusion and alloying steps are affected by the presence of variations in the doping density. Because of this, poor junction geometry and nonuniform current distributions are frequent problems in devices fabricated from inhomogeneous material. Device failures due to hot spots or thermal runaway may result.

Gross variations in resistivity also cause wide variations in device characteristics and contribute to poor device yields. As an example, a localized low resistivity region of a wafer limits operating voltages of a device fabricated from that wafer to values lower than those expected from the remainder of the wafer.

b. Limitations of Present Method

The method commonly used for determining the resistivity variation of starting wafers is the four-probe technique. There are several difficulties with this method. A basic limitation in the application of the four-probe method to the measurement of resistivity variations is the relative large sampling region of the probes [3]. Because of this, it has even been recommended that to obtain better spatial resolution, a two-probe measurement be made along a narrow bar cut from along the diameter of interest [4]. Also, there can be large errors introduced into the four-probe measurement due to slight mislocations of the probes [3,5]. Perhaps the biggest drawback of any probing method is the placing of probes on the wafer surface in precisely those areas where diffusions and other processing steps are to occur. The damage caused by the probes may of itself be detrimental to the reliability and yield of devices fabricated in these wafers. In addition, the method is very time-consuming

when used to obtain the variations in resistivity over an entire wafer diameter.

c. Photovoltaic Technique

The photovoltaic technique potentially offers an alternative for the measurement of resistivity variations along the diameter of circular silicon wafers. The technique, which is based upon the theory of Tauc [6], requires no contact upon the wafer surface area where a finished device or devices are to be fabricated.

The validity of a modified theory for circular geometry for the measurement of resistivity variations of circular silicon wafers using the photovoltaic technique was demonstrated some time ago [2], but the feasibility of this method for rapid, automated measurement of high-resistivity, large-diameter wafers remains to be demonstrated. It is the purpose of this task to determine this feasibility, and if feasible, to fully develop a prototype system.

d. Theory of Photovoltaic Effect

Tauc [6] has derived the underlying physical law of the photovoltaic phenomenon and has discussed its physical aspects. The bulk photovoltaic effect is a physical phenomenon which occurs when electron-hole pairs are photogenerated in a region of an impurity-density gradient. In the region of an impurity-density gradient, or equivalently a resistivity gradient, an internal electric field exists in the semiconductor. This is much like the situation at a *pn* junction, only one is concerned here with a much smaller electric field. When excess electron-hole pairs are generated in this region, they are separated by the internal electric field. The steady-state distribution of the separated carriers is such that the magnitude of the net internal field is reduced. It is the reduction in magnitude of the net internal field which results in the photovoltage which can be measured at contacts made to the specimen. It is possible to relate this measured photovoltage to the resistivity gradient in the region where the excess electron-hole pairs are distributed.

The physics of the photovoltaic effect in one dimension is described graphically in figure 1. Figure 1a is a representation of a typical resistivity profile often found in high resistivity Czochralski-grown silicon. Figure 1b shows the band structure for such a resistivity variation. Also figure 1b illustrates how the internal field (as manifested by the variation with position of the conduction and valence band edges) causes the photogenerated electron-hole pairs to be physically separated. Thus a local voltage dipole is created. This results in a voltage measurable at the edges of the specimen. If the light is scanned along the diameter, a voltage profile can be determined, as shown in figure 1c. If this voltage is integrated over position, assuming that the steady-state excess density of photogenerated carriers is constant (i.e., independent of position) and multiplying by a constant dependent only upon known ma-

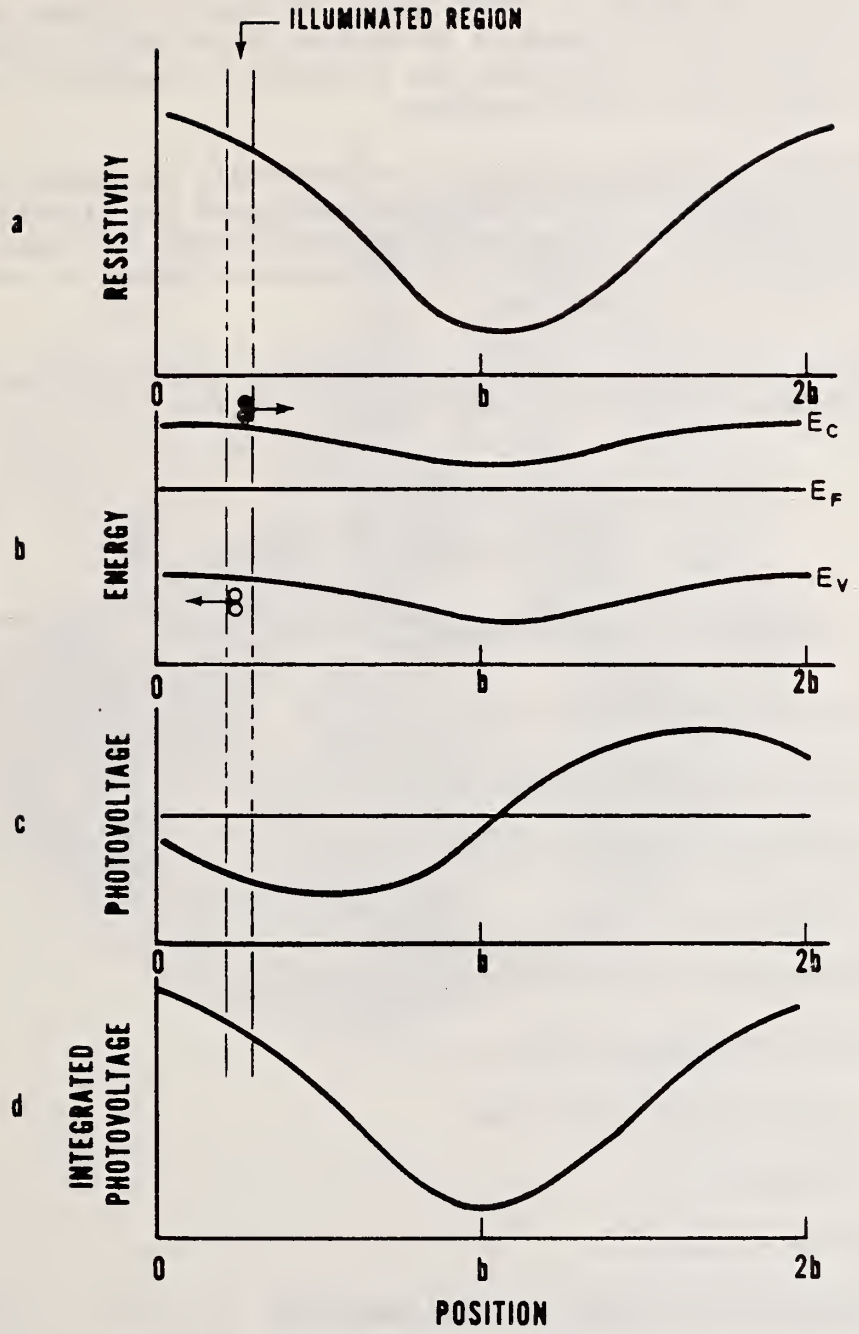


Figure 1. A representation of a (a) typical resistivity profile, (b) the associated energy band structure, (c) photovoltage, and (d) integrated photovoltage for an n-type silicon specimen.

terial parameters, one obtains the profile in figure 1d. This profile is identical to the variation in resistivity, as shown in figure 1a. Because the entire profile in figure 1d is shifted by an unknown integration constant, this method determines the variation in resistivity and not absolute resistivity at each position.

For most specimens, the excess density of steady-state photogenerated carriers is not constant. This is principally because the effective lifetime of the material is not constant but varies with position. This effect is accounted for by measuring the photoinduced change in specimen resistance as a function of position.

The equation that has been derived for relating the resistivity variation to the photovoltage for circular semiconductor wafers is [2]:

$$\frac{d\rho}{dx} = \frac{3q}{4\pi kT} \frac{(1 + \frac{\mu_M}{\mu_m})}{1 - (x/b)^2} \frac{\bar{\rho}^2}{bt} \frac{V(x)}{\Delta R(x)} \qquad (1)$$

where b and x are shown in figure 2 and

$\frac{d\rho}{dx}$ = resistivity gradient (Ω)

q = majority carrier charge (C)

K = Boltzmann's Constant (J/K)

T = temperature (K)

μ_M = majority carrier mobility ($cm^2/V \cdot s$)

μ_m = minority carrier mobility ($cm^2/V \cdot s$)

$\bar{\rho}$ = average resistivity ($\Omega \cdot cm$)

t = thickness (cm)

V(x) = photovoltage (V)

$\Delta R(x)$ = photoinduced change in resistance (Ω)

e. Measurement Procedure

To measure the resistivity gradient using the photovoltaic technique, the circuit shown in simplified form in figure 3 is used. First, the photovoltage as a function of position, V(x), is measured. This is done by having the switch S open, stepping the wafer beneath the light probe in constant increments, Δx, and measuring V(x) at each position.

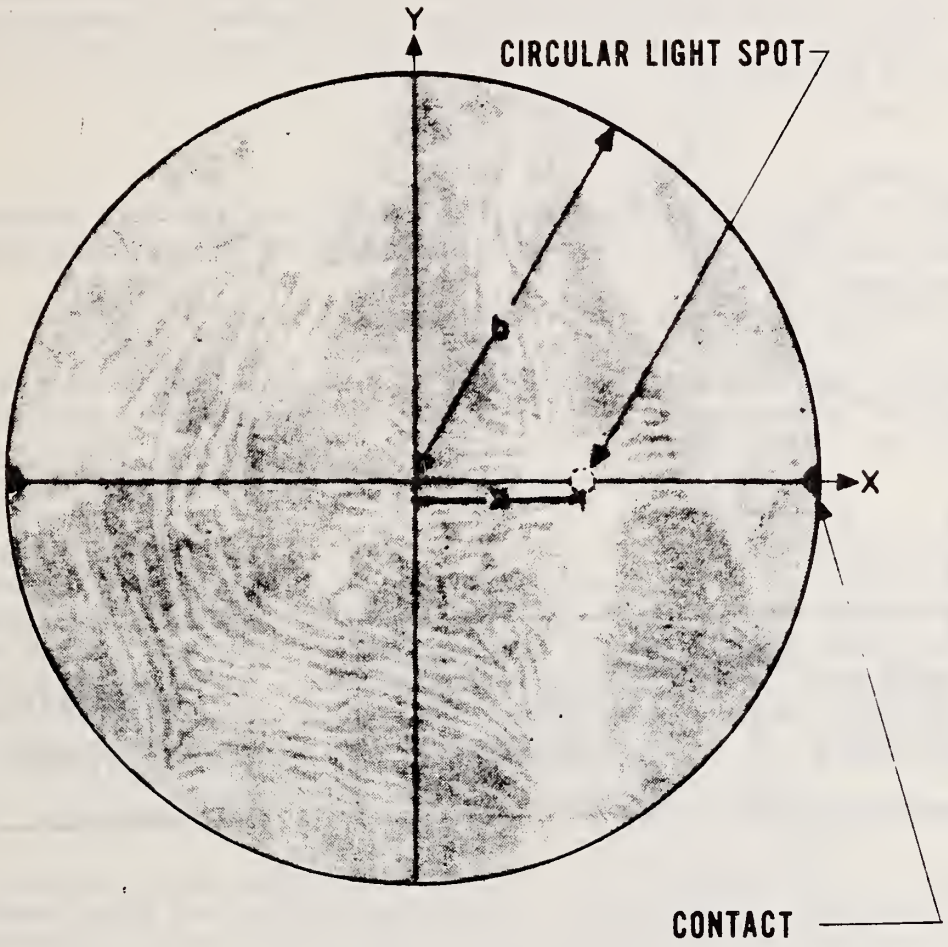


Figure 2. The wafer geometry upon which equation 1 is based.

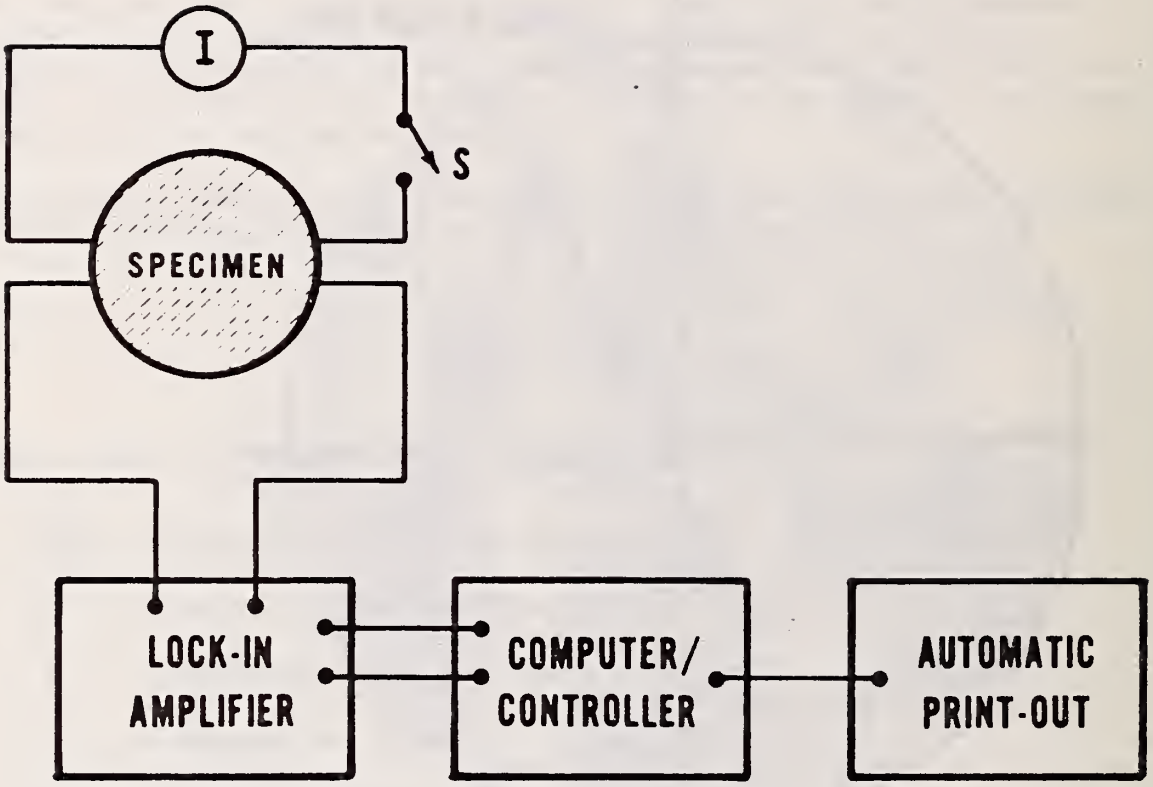


Figure 3. Simplified version of measurement system.

Next, the photoinduced change in specimen resistance, $\Delta R(x)$, is measured. This is accomplished by closing switch S and again stepping the wafer beneath the light probes in increments of Δx such that each $\Delta R(x)$ is measured at the same position as $V(x)$. Because a constant current, I, exists in the specimen with the switch closed, a decrease in the voltage across the specimen occurs as the light sweeps along the diameter. This is because the total specimen resistance is decreased due to the localized decrease in resistivity caused by the excess electron-hole pairs generated by the light. If the voltage is $\Delta V(x)$, then:

$$\Delta R(x) = \frac{\Delta V(x)}{I} .$$

The quantities $V(x)$ and $\Delta R(x)$ are then inserted in eq (1) to compute the gradient, $d\rho/dx$, at each position, x. To determine the variation in ρ, the plot of $d\rho/dx$ is numerically summed ($\rho_m(x) = \sum_{i=1}^{m} (d\rho/dx)_i \Delta x$). Thus a plot of the variation in resistivity is obtained. As mentioned, an absolute determination of resistivity is not obtained, but each $\rho_m(x)$ above differs from the absolute value by a constant, ρ_0, the value of the resistivity at the position the summation was begun.

The lock-in amplifier is used to extract the very low level photovoltage (typically 1 to 10 μV) from the background noise. The light source is chopped at a constant frequency (∿400 Hz) and the lock-in amplifier tuned to that frequency. The constant current for the measurement of $\Delta R(x)$ is supplied by a second pair of contacts to eliminate the difficulty of measuring small voltage changes with contacts carrying significant levels of current (∿100 μA to 1 mA).

2.3 Objective 1.1: Specimen Holders - Electrical Contacts

Two specimen holders were constructed. One holder, shown in figure 4, was based upon the knife-edge contacting arrangement previously demonstrated [2]. There are a number of problems associated with the knife-edge arrangement, most of which are mechanical. Principally, due to the design of the system, it was very difficult to assure that each knife edge of each pair contacted the wafer. It is also difficult to assure uniform contact over the entire thickness of the rim so that quite often only a point on the rim is contacted by each knife edge. Because of this, the edges of the wafer would sometimes be chipped. Also, the knife-edges themselves would often be chipped, further reducing the region of contact. This holder performed all of the requirements for centering the slice properly and if a system for ensuring good knife-edge contacts can be achieved, the design should prove workable.

Because of the problems with the knife-edge system a second specimen holder, shown in figure 5, was fabricated in which point probes replace the knife edges and the place of contact was moved from the rim to the top surface about 0.25 mm from the rim. This was done to try to take

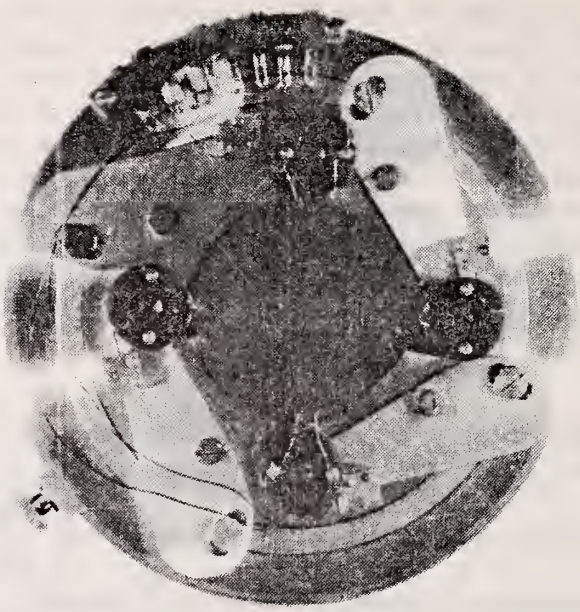


Figure 4. Photograph of knife-edge specimen holder.

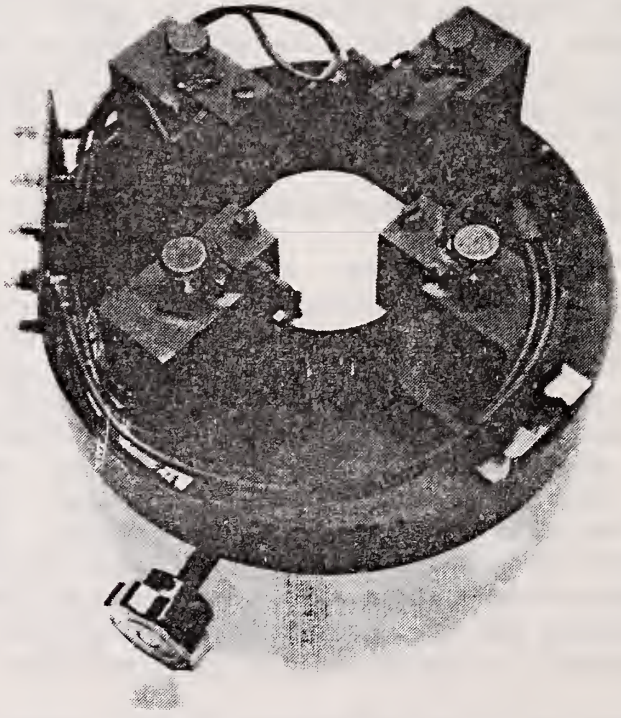


Figure 5. Photograph of point probe specimen holder.

advantage of the better known technology for making point probe contacts, such as used in four-probe and spreading resistance measurements. The proximity of the probes to the rim should permit eq (1) to be used unaltered, although this is yet to be established fully. In addition, any damage done by the probes to the surface should be inconsequential because it would be close to the rim in a region usually removed in the finished device.

Some comparisons of the current voltage (I-V) characteristics of the knife edges and the point probes are shown in figure 6. These curves are for two contacts in series. In each instance, the contact resistance for the point probe contacts is less than for the knife edges. The linearity of the relation is better for the point probes, indicating more ohmic contacts. It has also been found that the I-V characteristics of the point probes are more repeatable from wafer to wafer than that of the knife edges.

Because of the improved contact and ease of assuring good mechanical contact, the applicability of the point probes to the photovoltage measurement is now being determined. Concurrently, improved methods for making knife-edge type contacts at the wafer rim will be sought.

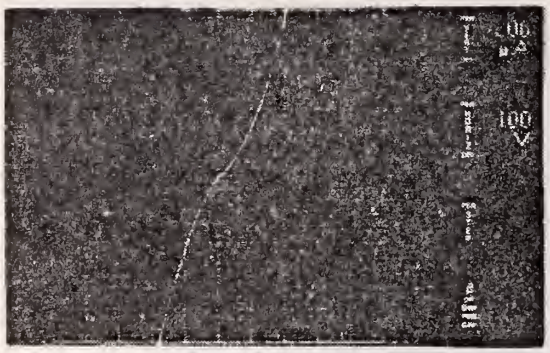
2.4 Objective 1.2: Automated Measuring System

A photograph of the automated system is shown in figure 7. An expanded block diagram is shown in figure 8. The various items, their functions, and some important features are listed in table 1.

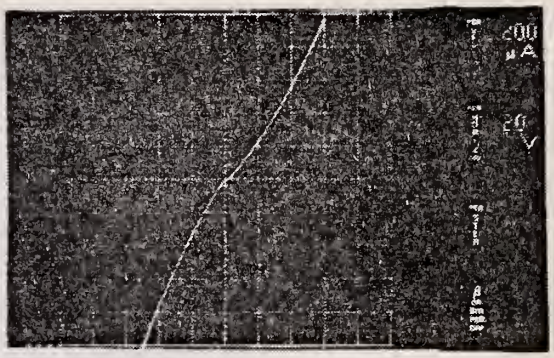
The system illustrated in figure 8 is designed to determine the resistivity variation along a diameter of a large-diameter silicon wafer by measuring the photovoltage between the points at which the diameter intersects the edges of the wafer. The wafer is then rotated 90 deg and a similar set of measurements made on the perpendicular diameter.

The wafer under test (W) is mounted in the wafer holder (H) which in turn is mounted on the motor-driven stages (L,R). Four sets of probes (K) make electrical contact with the periphery of the wafer near the ends of two perpendicular diameters but, for clarity, only two sets of probes are shown in figure 8. The wafer holder is oriented on the stages so that the wafer is concentric with the platform of the rotary stage and so that the movement of the linear stage is parallel to one of the diameters determined by the electrical contacts.

Photoexcitation is furnished by a horizontally mounted helium-neon laser, with a wavelength of 1.15 μm. The laser beam is directed to the center of the rotary stage by mirror M and produces a spot about 1 mm in diameter at the wafer surface. To improve the signal-to-noise ratio, the beam is chopped and the photovoltage is measured by a lock-in amplifier which is synchronized to the frequency of the chopped light beam. The chopping frequency (about 400 Hz) is adjusted so that the "on" time of the laser beam is long enough to achieve a steady-state excess-carrier distribution.

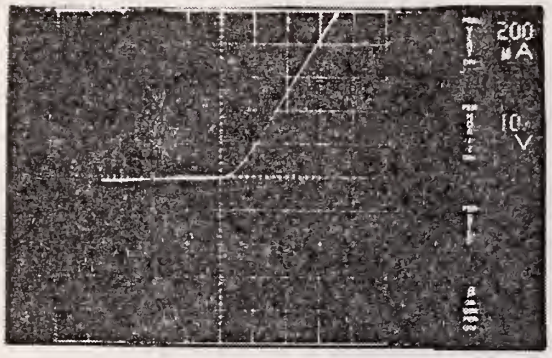


knife edge

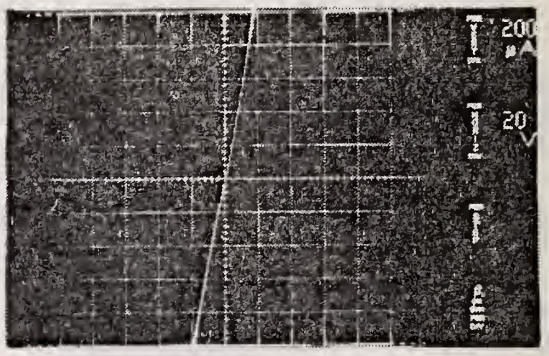


point probe

(a)



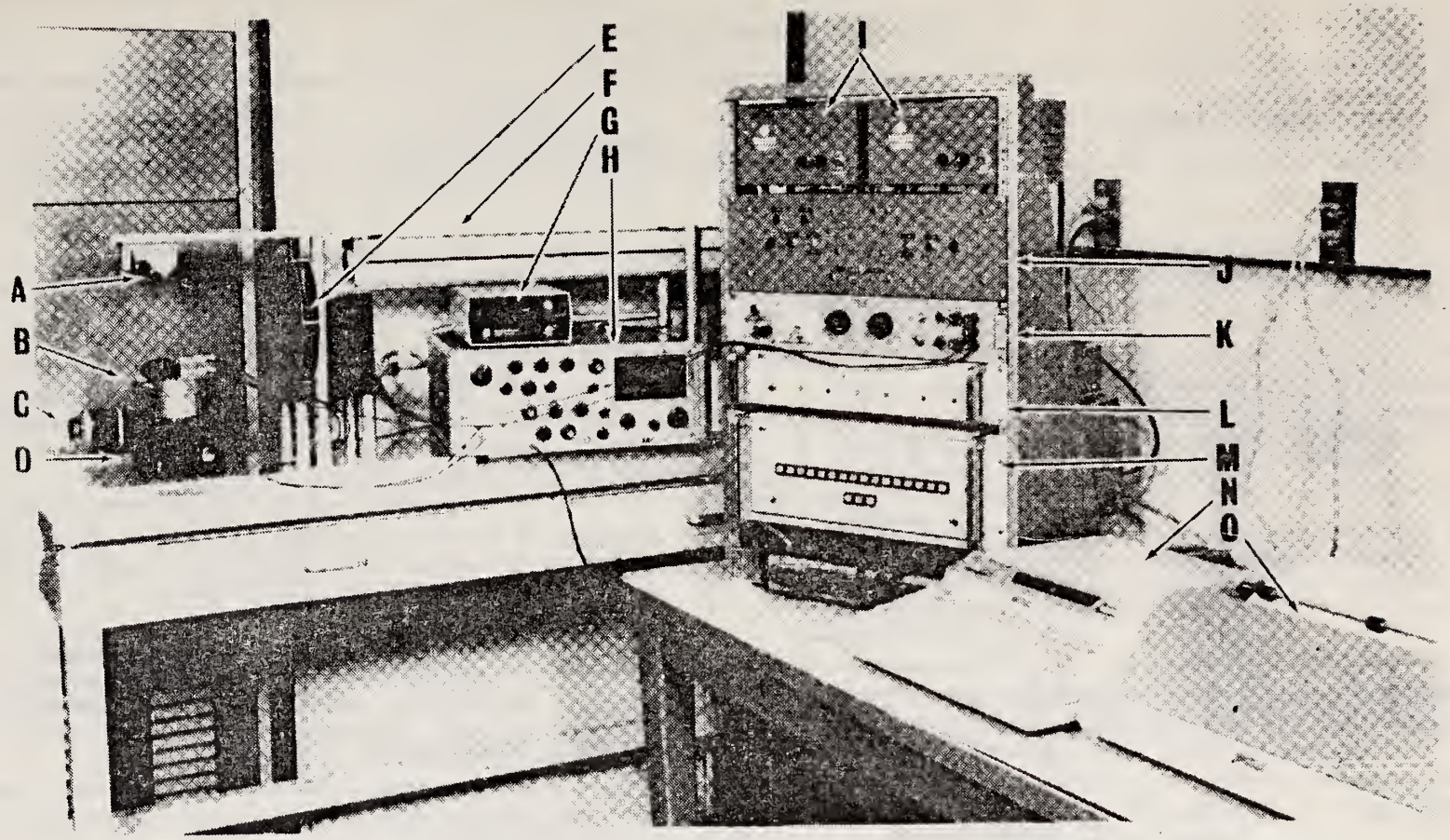
knife edge



point probe

(b)

Figure 6. Current-voltage (I-V) comparison between knife edges and point probes. (a) 150 Ω·cm n-type specimen, (b) 30 Ω·cm n-type specimen.



A - MIRROR
B - WAFER HOLDER
C - MOTOR-DRIVEN ROTARY STAGE
D - MOTOR-DRIVEN LINEAR STAGE
E - LIGHT CHOPPER
F - He-Ne LASER
G - LASER POWER SUPPLY
H - LOCK-IN AMPLIFIER
I - STEPPING-MOTOR TRANSLATORS
J - MOTOR CONTROL PANEL
K - CONSTANT-CURRENT SUPPLY
L - MULTIPROGRAMMER INTERFACE
M - MULTIPROGRAMMER
N - CALCULATOR/CONTROLLER
O - PRINTER/PLOTTER

Figure 7. Photograph of automated system.

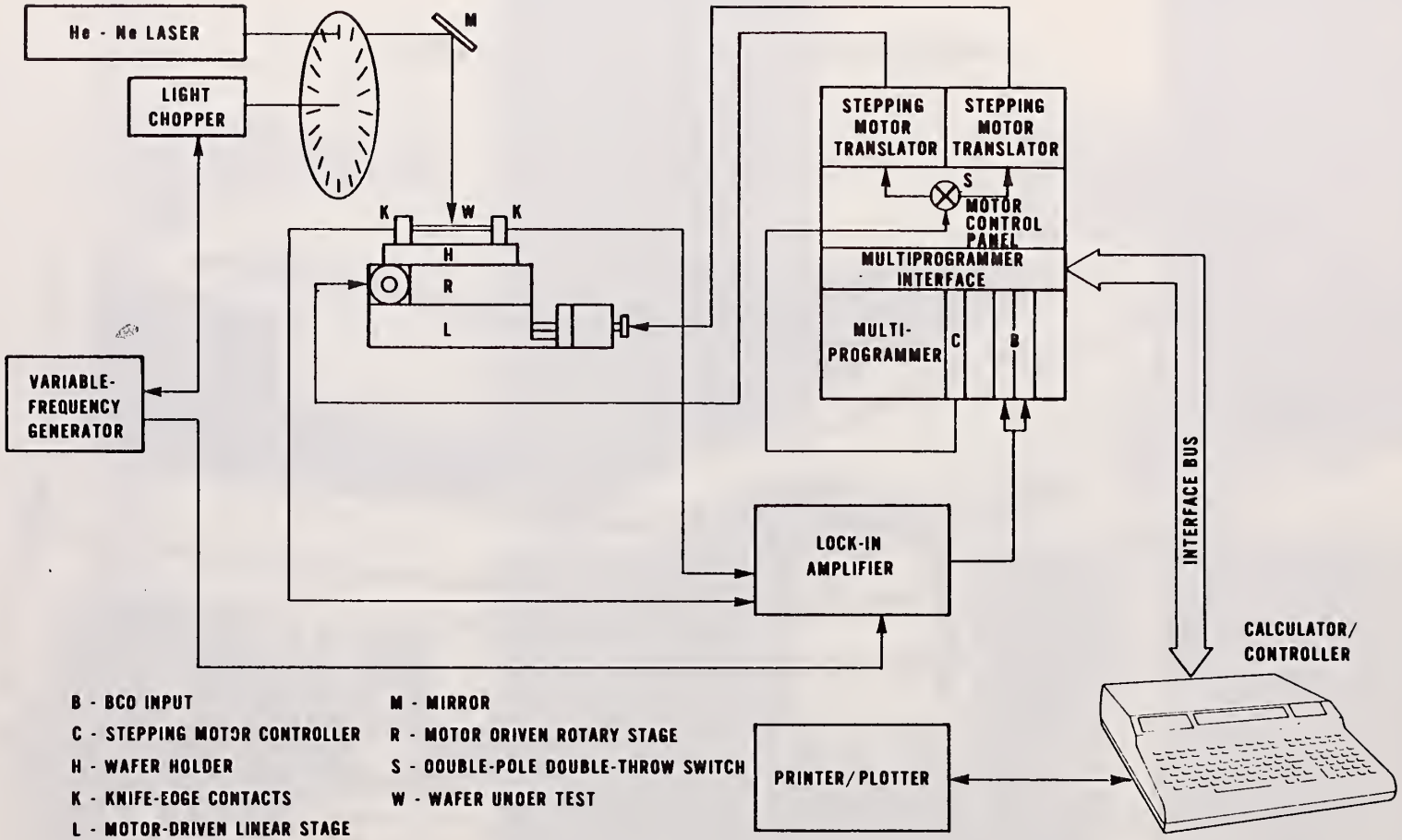


Figure 8. Schematic of automated system.

Table 1 - Equipment for Resistivity Profiling

ITEM	FUNCTION	SOME IMPORTANT FEATURES
Laser	To provide source of energy to generate electron-hole pairs - replaces incandescent light source used in earlier work [2].	He-Ne; >2-mW power at 1152-nm output.
Lock-In-Amplifier & Light Chopper	Light chopper chops light at constant frequency and lock-in amplifier monitors signal at that frequency. Permits low level ($\sim$1-μV) signals to be measured.	High input impedance (100-MΩ) differential preamplifier; sensitivity to 100-nV full scale; digital read-out; BCD output; programmable functions.
Linear & Rotary Motor Driven Stages	To translate wafer to be measured beneath laser probe and to permit 0-180° rotation of wafer.	Total linear travel - 85 mm; linear resolution - 0.01 mm; linear bidirectional repeatability - 0.005 mm; rotational resolution - 2 arc minutes; rotational bidirectional repeatability - 0.2 arc minutes.
Multiprogrammer	Distributes instructions from controller to instruments, acquires data and multiplexes it to the computer/controller.	Part of the computer/controller system; compatable with IEEE Standard Digital Interface for Programmable Instruments - IEEE Std. 488-1975.
Computer/Controller	Controls system, reduces data, controls printer/plotter to permit output of data.	Programmable; compatable with IEEE Std. 488-1975.
Printer/Plotter	To provide hard copy of measured resistivity profile.	Alpha-numeric plotter; compatable with IEEE Std. 488-1975.

The wafer is scanned by moving it under the stationary laser beam. Movement of the stages and measurement of the BCD (Binary Coded Decimal) output of the lock-in amplifier are under the automatic control of the calculator/controller, which records the data, performs the required calculations to convert photovoltage to resistivity, and plots the results if desired.

The calculator/controller communicates directly with the printer/plotter, and with the lock-in amplifier and stepping motors through the interface bus and multiprogrammer. Under the direction of a program stored internally or on magnetic tape, the calculator/controller:

1. Moves the linear stage under the laser beam so that the beam scans a diameter of the wafer under test.

2. Stops the stage at predetermined points along the diameter.

3. Directs the lock-in amplifier to read the voltage at each point.

4. Records the data on the printer/plotter either in voltage or as resistivity, and if desired, stores the results in memory for later use in plotting or for other purposes.

After measurements of the photovoltage and photoinduced change in resistance along the first diameter are completed, the wafer is rotated 90 deg and the measurements repeated.

Under the direction of the calculator/controller, the stepping motor control card (C) in the multiprogrammer generates a pulse train of the required length to move the motor the desired number of steps in either the clockwise or the counterclockwise direction. The output of the card is applied to one of the translators through a switch (S) which selects either the linear or the rotary stage. The translators apply the pulses to the stepping motor windings in the proper sequence and with sufficient power to drive the motors. Each pulse advances the linear stage 0.01 mm or rotates the platform of the rotary stage 2 arc minutes.

The rotary stage is continuously rotatable, but the linear stage has limited range. When the linear stage reaches either end of its travel, it causes a switch to close. To avoid damage to the stage when this point is reached, the switch is used to interrupt the signal to the motor by means of a relay in the motor control panel. Simultaneously, a light on the panel indicates which limit has been reached. The motor control panel also contains switches for manually moving the stages one step at a time. The control panel wiring diagram is shown in figure 9.

The BCD output of the lock-in amplifier is transmitted to the calculator/controller through the BCD input cards (B) in the multiprogrammer. Two cards are required to furnish the 18 lines needed for 13 bits of data, 3 bits to indicate scale, and one bit each for polarity and overload.

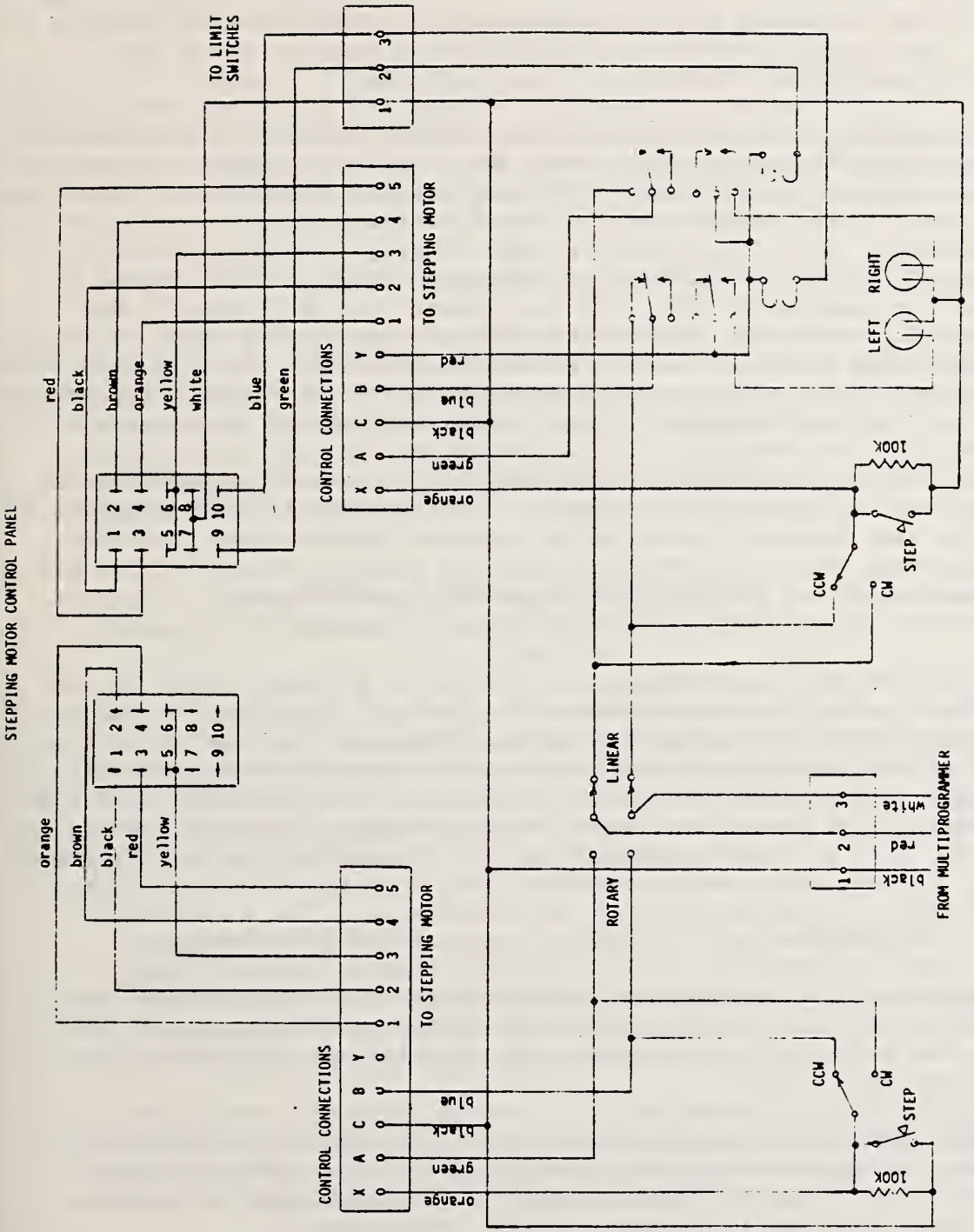


Figure 9. Schematic of stepping-motor control module.

All measurements are controlled from the keyboard of the calculator/ controller or from programs which are either stored in the calculator/ controller or read into it from tape cassettes. A typical program for the measurement of photovoltage or photoinduced resistance change along perpendicular diameters begins with the laser beam at the center of the wafer. The center is used as a reference point since it is an easy point to identify and is common to both diameters.

At the beginning of the program, the operator is directed to enter wafer identification, the wafer diameter and thickness, its average resistivity, the number of measurements to be made on each diameter, the distance between measurements, and the duration of the pause to allow for meter settling time before taking a meter reading. Following this, the measurements along the diameter are made automatically. The program determines the location of the first measurement from the number of measurements to be made and the distance between measurements and positions the wafer under the laser beam at this starting point. The voltage across the wafer is then read and recorded. The wafer is then moved the prescribed distance, typically 1 mm, along the diameter, and after a pause to allow the reading to settle the voltage is again read and recorded. This is repeated until the prescribed number of measurements has been made along the first diameter. The sequence is then repeated along the same diameter, but with the constant current source switched on. Following this set of measurements, the wafer is rotated 90 deg and the measurements are repeated on the perpendicular diameter. A typical program with an explanation of its features is included in Appendix A.

The results of these measurements are printed in a double column as they are made to permit the measurements to be checked. The first column records the location of the laser beam in millimeters from the center of the wafer, and the second column lists the voltage measured across the wafer when the laser beam is at that position. Wafer identification and the conditions of measurement appear as a heading at the top of the columns. The data are also stored for use in calculations or for plotting voltage or resistivity versus distance along a particular wafer diameter.

2.5 Objective 2.1: Measurements and System Evaluation

Measurements of photovoltage and photoconductivity with the system have just begun. A number of difficulties in making these measurements have arisen, but sufficient measurements have not been made to identify and isolate specific causes.

The major difficulties are (1) the presence of a "transverse" photovoltage, that is, a photovoltage measured between the two contacts at the same end of the diameter being scanned and (2) the inability to consistently make reproducible photoconductivity measurements.

It has not been established if the "transverse" photovoltage is a true bulk photovoltage effect or caused by some anomaly occurring at the contacts such as scattered light generating a voltage at the metal-silicon contact. The problems with the photoconductivity measurements have gen-

erally been associated with the negatively biased current carrying contact on *n*-type silicon. This could be caused in some way by the barrier at this metal-semiconductor contact or perhaps even be associated with the above mentioned "transverse" photovoltage.

The major differences between the present electrical measurement system and that previously used [2] are (1) the point probes replacing the knife edges, and (2) the infrared laser (1.15 μm) replacing the visible light source. The 1.15-μm light was chosen to give a more uniform generation of electron-hole pairs with depth. The effect of these changes as related to the above problems is now being investigated.

2.6 Objective 2.2: Documentation for Photovoltaic System

The effort under this objective will be to write a manual detailing the construction of the photovoltaic scanning system, including applicable engineering drawings and system and component specifications. Operation of the system will be explained with step-by-step procedures.

If appropriate, a videotape may be produced describing the system and its application and demonstrating it in actual operation.

3. THERMALLY STIMULATED MEASUREMENTS

3.1 Objectives

The overall objective of this task is to evaluate the use of thermally stimulated current and capacitance measurements as a means for characterizing defects in power grade silicon material. Thermally stimulated current and capacitance (TSM) are used to identify and characterize deep level defect centers in the band gap of silicon. Phase 1 of the task, January to September 1976, had the following objectives:

1.1 Develop a suitable technique for evaluating starting material using thermally stimulated current and capacitance measurements on metal-oxide-semiconductor (MOS) capacitors; a key to this objective is the ability to fabricate MOS structures with low temperature oxides (in order to preserve the characteristics of the starting material) and their evaluation.

1.2 Design and construct apparatus for performing thermally stimulated current and capacitance measurements on large-diameter silicon wafers in the appropriate temperature range and evaluate the low temperature oxide samples using TSM.

1.3 Determine the feasibility of using and interpreting TSM on thyristors after each step in the device fabrication process; this objective involves direct interaction with manufacturers of devices to obtain general information on processing procedures as well as to establish sources of material and devices.

Phase 2 of the task, October 1976 to October 1977, has the following objectives:

2.1 Develop procedures for the fabrication of MOS capacitors and *pn* junction structures on in-process (diffused) power thyristor wafers to allow characterization of defects in processed material.

2.2 Utilize TSM to detect defects in processed power device material, and examine various interferences which could obscure or distort the defect response.

2.3 Establish the transient capacitance technique as an adjunct to the conventional stimulated current and capacitance measurements, and evaluate the feasibility of using TSM for defect (lifetime) profiling.

To date, efforts have been made in each of the objective areas. The objectives of Phase 1 have been met; the work of Phase 2 is presently continuing and is expected to be completed on schedule. This report will discuss the progress that has been made toward each of these objectives.

3.2 Background

Thermally stimulated current and capacitance measurements [7-11] utilize the ability of active defects in depletion regions to trap majority carriers and to emit them after receiving sufficent thermal energy. Suitable analysis of the data allows determination of the density, energy level, and emission rate of the defect. Specific defects such as heavy metal contamination, irradiation-induced defects, and process-induced defects have been identified by various workers and each defect is noted to have a particular signature. The utility of the TSM technique lies in its ability to identify particular defects or contaminants by their characteristic signature. When fully developed, this capability will be a valuable tool for the process engineer to identify and monitor the presence of unknown defect centers which could degrade device performance. By the same token it can be used to monitor the presence of known or purposely introduced defects to tailor or control the lifetime of minority carriers.

The basic theories and principles underlying the TSM technique are understood and documented in the literature. For this reason a detailed discussion is omitted in the text of this report. However, for convenience, a tutorial article written by M. G. Buehler [9] describing the mechanisms which govern the TSM response is reprinted in Appendix B.

3.3 Objective 1.1: Low Temperature Processing for MOS Capacitors

The objectives of this study were to develop a test structure and a procedure for using the TSM technique to detect defects in silicon starting wafers. Three different types of oxide fabrication procedures were used with the goal of processing MOS capacitors using the lowest temperature

treatments. The process yielding the most consistent devices utilized chemical vapor deposition (CVD) of SiO_2 at 400°C along with a 400°C microalloy treatment.

The evaluation of starting material can be meaningful only if the fabrication procedures themselves do not alter the properties of the defects that are to be detected. Hence, an important requirement of the test structure fabrication procedure is the minimization or the elimination of high temperature process steps. The TSM method is equally applicable to either the *pn* junction or the MOS capacitor [10]. However, the necessity of a high temperature diffusion makes the junction unsuitable for use in starting material evaluation. The MOS capacitor, by virtue of its simple structure and fabrication procedure, is ideal for this purpose.

The general procedure for the fabrication of MOS capacitors includes the following steps:

1) wafer clean-up

2) application or growth of insulating oxide

3) application and photolithographic definition of gate metal on top side (level 4 of NBS-3 test pattern [12])

4) back side metallization for ohmic contact to substrate

5) microalloy of metallizations

Of these, only steps 2) and 5) involve temperatures substantially above room temperature (i.e., T > 120°C). Depending on the process chosen, the oxide formation step could range in temperature from 25°C to over 1000°C. Microalloy of metallization (typically 500°C) is used to enhance the adhesion of the gate metal to the oxide as well as to improve the ohmic contact to the substrate. In the case of aluminization by e-gun evaporation, the microalloy step also serves to minimize interface states induced by the X-radiation produced in the e-gun evaporator by the high energy electrons striking the evaporant material. For these reasons, efforts in the development of a process for MOS capacitors have been centered on the oxidation and the microalloy steps. The fabricated MOS capacitors were analyzed by measuring the capacitance-voltage (C-V) characteristics and comparing them to theoretically calculated [13] C-V curves.

a. Oxidation Procedures

Three different "low" temperature oxides were considered and compared with high temperature thermal oxide. Briefly, they can be characterized by the following:

1) anodic oxidation of the silicon wafer at room temperature

2) chemical vapor deposition (CVD) of SiO_2 onto the silicon wafer at 400°C

3) the complete oxidation at 400°C of tantalum metal evaporated onto the silicon wafer to form Ta_2O_5

Dry thermal oxidation at 1000°C was used as a "reference" standard for these studies since the properties of MOS capacitors fabricated with this procedure are well understood.

Figure 10 displays typical measured C-V curves for each of the oxide types fabricated. Calculated theoretical [13] curves are shown for comparison; these points have been shifted along the voltage axis to allow coincidence of V_{fb} (flat-band voltage) with the experimental curve. The SiO_2 capacitors (a, b, and d) show similar characteristics in that the flat-band voltages are all negative (indicating a positive surface state charge) and that the experimental curve lies above the theoretical one in the inversion region (indicating slight interface state dispersion). By contrast, the tantalum oxide specimen (c) shows a negative surface state charge and the theoretical curve shows higher dispersion than the experiment. Since this Ta_2O_5 specimen was very thin, the C-V measurement may not be valid because of the possibility of leakage in the oxide. If excess leakage occurs, the device may go into deep depletion rather than to true inversion, and the theoretical curve would not necessarily match the experimental curve.

A second group of Ta_2O_5 wafers with oxide layers about 0.08 μm thick (as compared with 0.03 μm for the first) also proved to be leaky and failed to produce capacitors suitable for TSM. Recent measurements by Kaplan, *et al.* [14] on CVD Ta_2O_5, indicate that tantalum pentoxide is intrinsically more highly conducting than typical thermal or CVD SiO_2, and therefore would not be expected to be suitable for the MOS structures required for this study. Hence, further investigation of Ta_2O_5 was discontinued. However, the C-V characteristics for all three SiO_2 specimens shown in figure 10 indicate that these devices would be satisfactory for the TSM technique.

An important consideration in the processing of test structures for a study of this type is the ability to reproducibly fabricate wafers with similar properties. In addition, it would not be convenient if the fabrication procedure introduces excessive "features" of its own which may interfere with the properties of interest. The CVD SiO_2 method qualifies adequately in both respects. In the process using anodic oxidation, it was found that successive processing runs failed to result in reproducible characteristics. The problem was traced to the inability to control the moisture content of the electrolytic solution. Success of the CVD oxide makes further studies of the anodic oxide unnecessary; however, this study will be resumed if it is found that a room temperature process is required.

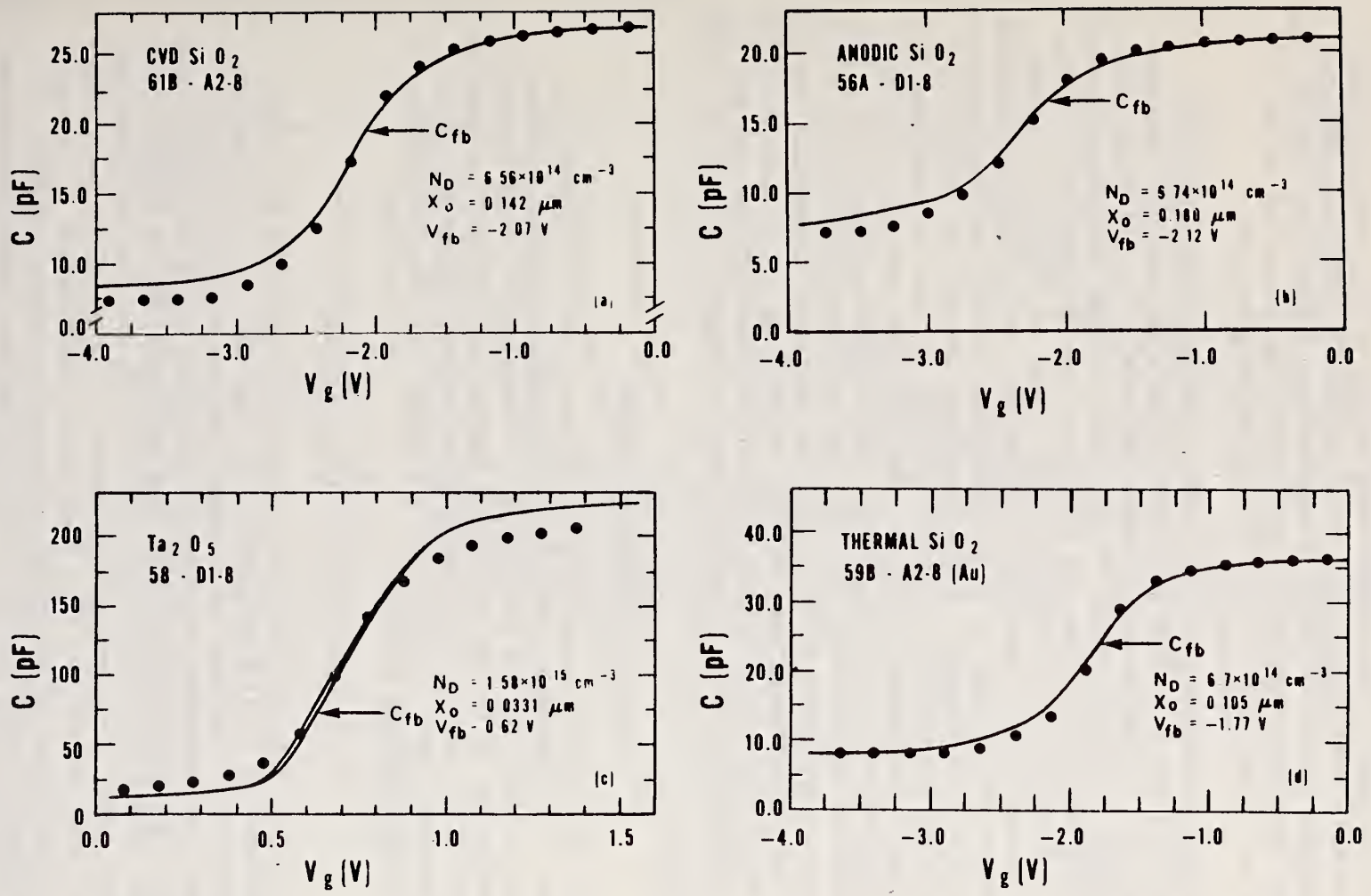


Figure 10. Measured C-V characteristics for four different oxides (n-MOS): (a) chemical vapor deposited SiO_2, (b) anodically grown SiO_2, (c) oxidized tantalum - Ta_2O_5, and (d) thermally grown SiO_2; theoretical curves are shown as dots.

b. Microalloy Temperature Variations

Using the CVD procedure, the highest temperature that a starting wafer encounters with the described fabrication procedure is the microalloy step. Since this occurs at 500°C, a temperature higher than that of the CVD oxidation process, a series of experiments was conducted to see if a lower microalloy temperature produced acceptable devices.

Four wafers were processed with dry thermal oxides (oxide thickness, $X_o \simeq 0.09$ μm). After gate metallization (e-gun aluminum) and photoengraving, each of the four wafers was microalloyed at a different temperature for 20 min in dry nitrogen. Capacitance-voltage measurements were made on the MOS capacitors, and the results of the measurements on four capacitors from each of the four wafers are shown in figure 11. Wafer 74A was not microalloyed at all and it shows the typical large interface state distortion accompanied by the higher than normal flat-band voltage shift due to the X-ray damage. Since interface states can contribute interferences, their presence in wafer 74A make it less satisfactory for TSM. The other three wafers, 74B, 74C, and 74D show very little interface state distortion but varying quantities of oxide charge (Q_{ss}). The characteristics of samples 74B, 74C, and 74D would be satisfactory for the TSM technique providing that Q_{ss} remains stable as is usually the case. This result indicates that a 400°C microalloy for 20 min in dry nitrogen of e-gun aluminized wafers produces satisfactory devices and thus would be compatible with the 400°C process required by the CVD SiO_2 fabrication.

c. A Suitable MOS Process

Table 2 gives the procedure used for fabricating the low temperature MOS capacitor. The processing steps are conventional and are typical of planar silicon fabrication facilities. The two 400°C heat treatment steps are considered to be low enough in temperature to avoid alteration of the native defect density, or introduction of new defect centers. This is the process that is currently being used for the fabrication of MOS capacitors on starting wafers.

3.4 Objective 1.2: Wafer Apparatus

The thermally stimulated current and capacitance technique is established and documented [7-11], but until the beginning of this contract, all measurements had been made on packaged devices scribed from processed wafers. The necessity to scribe, die bond, and wire bond devices into packages unnecessarily lengthens the time required to analyze processing steps. One objective in this study is to use the TSM technique on whole wafers; such a technique eliminates all steps after wafer fabrication and allows relatively fast feedback of information to the process line. In addition, application to the power device industry requires wafer handling capabilities since devices are generally the size of the entire wafer. This approach requires the development of a large-area, thermally controllable chuck, optimized for its thermal response. To accommodate these needs, a thermal chuck was designed and incorpo-

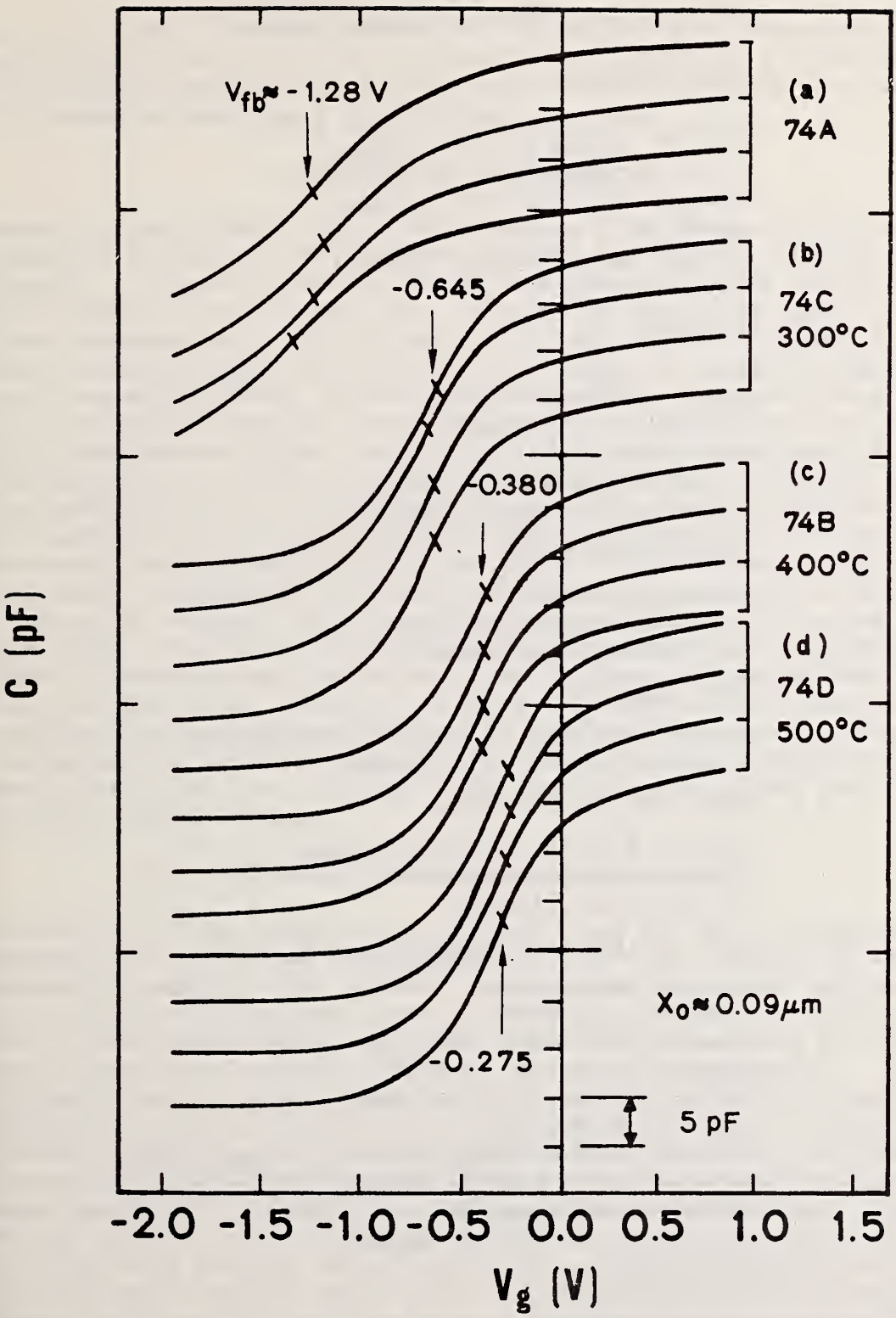


Figure 11. C-V characteristics of four wafers treated at different microalloy temperatures: (a) no microalloy, (b) 300°C, (c) 400°C, and (d) 500°C. (The vertical scale applies only to the lowest curve; the others have been displaced vertically for clarity; the oxide capacitance is about 45 pF.)

Table 2 — Basic MOS Fabrication Process

1. Wafer Cleanup

   1:1:2 $NH_4OH:H_2O_2:H_2O$ 20 min @ 50°C
   DI-H_2O 10 min @ 23°C (rinse)
   1:1:2 $HCl:H_2O_2:H_2O$ 20 min @ 50°C
   DI-H_2O 10 min @ 23°C (rinse)
   1% HF 30 s @ 23°C
   DI-H_2O 10 min @ 23°C (rinse)
   Blow dry with N_2

2. CVD-SiO_2

   N_2: 20 sLpm
   O_2: 0.025 sLpm
   4% SiH_4/N_2: 0.28 sLpm
   400°C substrate
   0.04-μm/s deposition rate
   0.15-0.25-μm final thickness

3. Gate Metallization

   aluminum (e-gun)
   0.005-μm/s deposition rate
   0.5-μm final thickness

4. Back Side Etch

   expose back side to vapors of 48% HF
   DI-H_2O 10 min @ 23°C (rinse)

5. Back Side Metallization

   gold (+ 0.6% Sb) (thermal source)
   0.004-μm/s deposition rate
   0.2-μm final thickness

6. Gate Metal Photolithography

   spin-on photoresist
   bake 20 min @ 75°C
   expose 20 s (NBS-3, level 4)
   develop 30 s
   DI-H_2O 10 min @ 23°C (rinse)
   bake 20 min @ 120°C
   etch Al 20:5:1 $H_3PO_4:H_2O:HNO_3$ 8 min @ 23°C
   DI-H_2O 10 min @ 23°C (rinse)
   strip resist (acetone)
   DI-H_2O 10 min @ 23°C (rinse)

7. Wafer Cleanup

   repeat step 1.

8. Microalloy

   N_2: 0.25 sLpm
   20 min @ 400°C

rated into a modified wafer probing apparatus. It has a temperature range from 79 K to 623 K with a heating rate in excess of 6.5 K/s and has been used to measure currents as small as 200 fA (0.2 pA) and capacitance changes as small as 5 fF (0.005 pF).

a. Thermal Chuck Requirements

A thermally controllable chuck capable of providing the necessary temperature conditions for the TSM technique has a number of critical requirements. The basic ones are listed in table 3. The low temperature limit is fixed by the coolant used; in this case liquid nitrogen, which boils at approximately 77 K, is used. The high temperature limit is fixed by the mechanical and material capabilities of the chuck components: excessive thermal expansion or contraction, excessive power density in the heater elements, excessive oxidation of surfaces, etc. Typically, temperatures higher than 350°C (623 K) are not required. The amplitude of the thermally stimulated current response is proportional to the heating rate [7]; hence, it is desirable to have the highest possible heating rate. A high cooling rate is also desirable to minimize turn-around time in the cycling of the system. Good thermal isolation of the chuck is important to prevent unnecessary heating and cooling of the supporting hardware and to maximize heat transfer to the active area of the chuck. Electrical isolation of the chuck surface is necessary in order to measure small currents and small change in capacitance. Mechanical motion of the chuck due to thermal expansion and contraction during heat cycling must be minimized to reduce relative motion between the wafer and the probes. Finally, the chuck should accommodate large-diameter wafers and have a vacuum chuck to hold the wafer for good electrical and thermal contact.

b. The Thermally Controllable Wafer Chuck

Consideration of the requirements outlined above led to the design and construction of the thermal chuck shown in figure 12. Figure 12a shows a schematic diagram of the component parts of the chuck; the various parts are identified and are listed numerically in table 4. The top plate (3) has vacuum grooves for wafer hold-down, a deep hole for thermocouple insertion and mounting holes for the wafer index-stop (2). The top plate is nickel-plated copper and is electrically isolated from the chuck body (5) by the insulator plate (4); the use of mica, 0.025-mm polyamide, or 0.25-mm sapphire for this insulator plate were considered. This insulator must provide good electrical isolation as well as good thermal conduction. Of the three, the sapphire plate was found to perform most satisfactorily and is in current use. The heart of the assembly is the chuck body (5) which consists of an integral cooling cavity and holes for the heater cartridges (10). An inverted view of this part is shown in figure 12b, with the heaters exposed. The cover plate (6) encloses the cooling cavity and attaches to the manifold (9) for the coolant fluid. The heater cartridges (10) (150 W each) are silver-soldered into the copper chuck body (5); the chuck body is subsequently heli-arc welded to the stainless steel cover plate (6) and mounting ring (7). Since the mounting ring (7) is attached to supporting hardware, it

Table 3 — Thermal Chuck Attributes

1. Temperature Range

   80 K to over 600 K

2. High Heating Rate

   >6 K/s

3. High Cooling Rate

   (For rapid turn-around time)

4. Thermal Isolation to Minimize Heat Transfer to Supports

5. Electrically Isolated Thermal Surface

   DC isolation for picoampere measurements
   AC isolation for picofarad measurements

6. Appropriate Shielding to Minimize Noise Pickup

7. Minimal Mechanical Motion of Chuck During Thermal Cycling

8. Vacuum Chuck Wafer Hold-Down Capability

9. Large Diameter Wafer Capability

   4 in (100 mm) or greater

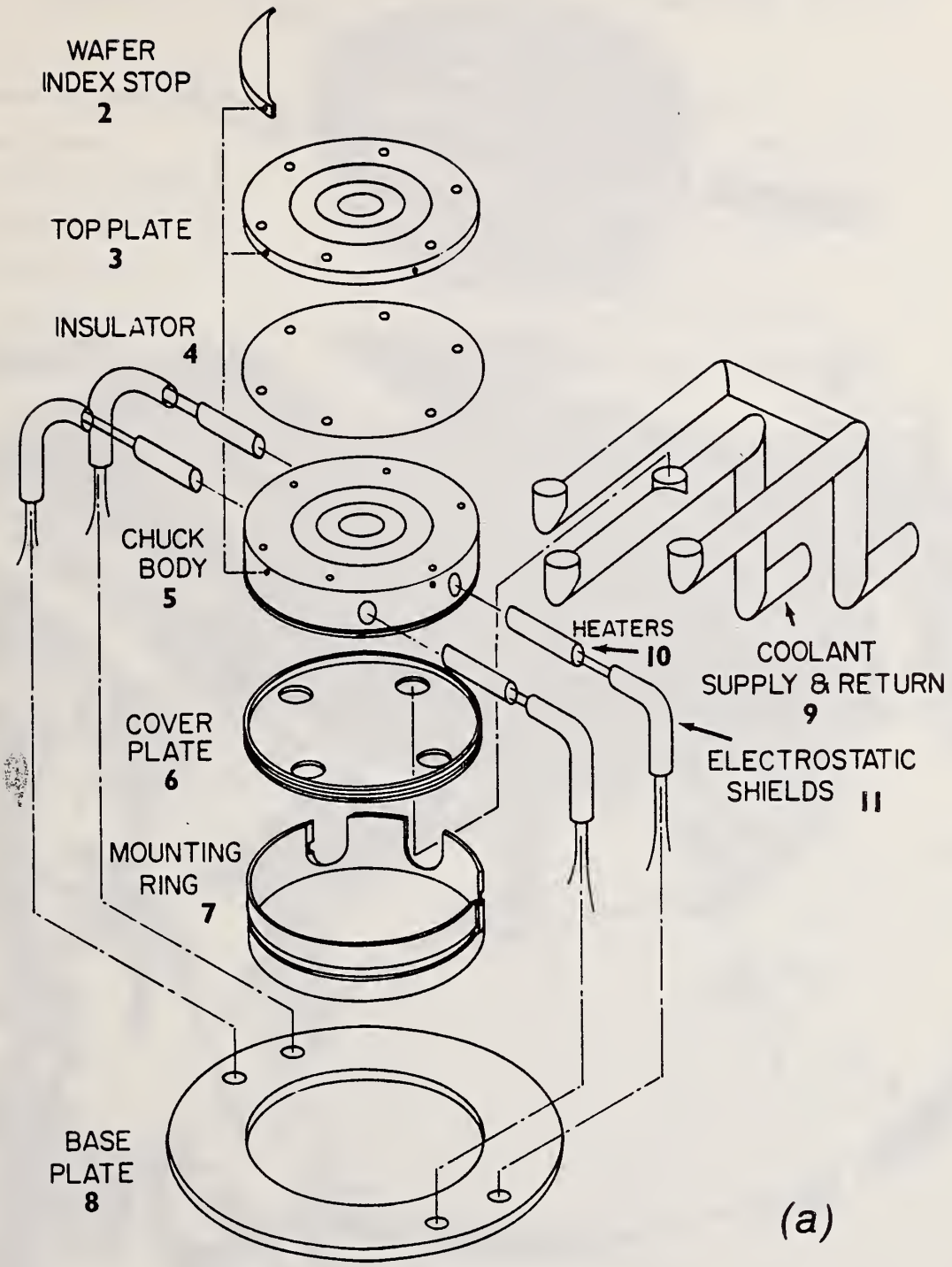


Figure 12. The thermal chuck assembly: (a) Detailed view of the major components. (The numbers indicate major components of the assembly listed in table 4.)

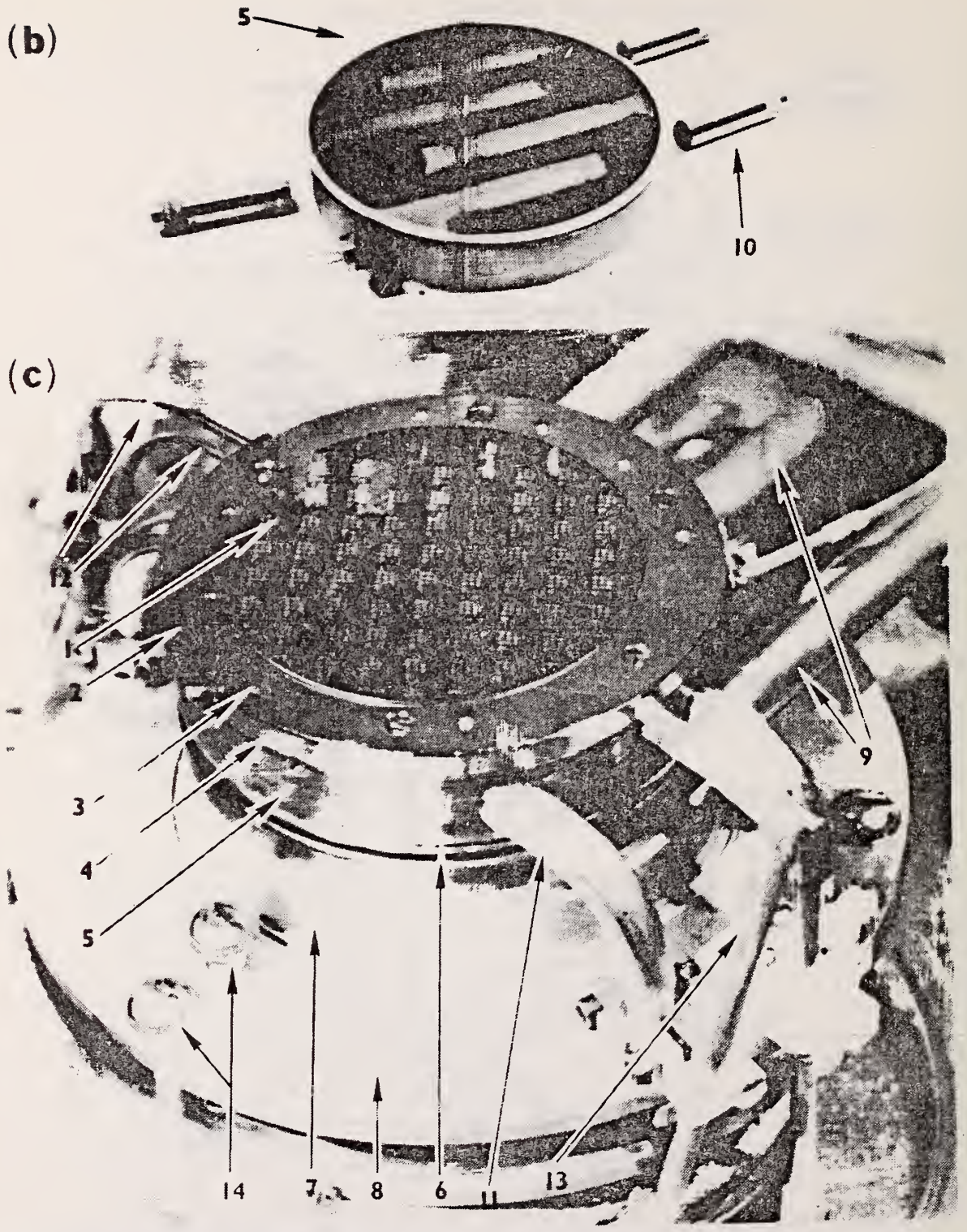


Figure 12. The thermal chuck assembly: (b) Inverted view of the chuck body with the heater cartridges exposed. (c) Photograph of the assembled thermal chuck. (The numbers indicate major components of the assembly listed in table 4.)

Table 4 — Component List for Thermal Chuck and Wafer Probing Apparatus

1. 2-in (50-mm) wafer
2. Wafer index-stop
3. Top plate
4. Insulator plate
5. Chuck body
6. Cover plate
7. Mounting ring
8. Base plate
9. Coolant manifold (2 ea.)
10. Heater cartridge (4 ea.)
11. Electrostatic shield (4 ea.)
12. Thermocouple (2 ea.)
13. Chuck vacuum supply (2 ea.)
14. Leveling and locking screws (3 pr.)
15. Probe ring height manipulator
16. Stereo microscope
17. Prober control panel
18. Top viewport
19. Wafer transfer probe
20. Wafer θ-alignment manipulator
21. Microscope mounting post
22. Wafer transfer slide
23. Front viewport
24. Prober control connector
25. Liquid nitrogen feedthrough (2 ea.)
26. Dry nitrogen feedthrough (2 ea.)
27. Heater power, thermocouples, etc.
28. Prober bridge assembly
29. Probe ring height micrometer
3. Probe ring support
31. Multiprobe assembly
32. Probe ring
33. Probe and manipulator (6 ea.)
34. Telescoping tubes/stainless steel bellows

has been designed with a thin rib (0.25 mm) on the circumference to minimize heat transfer to the support. The power leads for the heater cartridges (10) are shielded along their entire length with either solid (11) or flexible metal shields. The top surface of the chuck body (5) is identical (including vacuum grooves) to the top plate (3); for measurements which do not require electrical isolation this feature will allow higher thermal response. Figure 12c shows a photograph of the assembled thermal chuck. The two independent thermocouples (12) are seen near the top of this photograph; although not necessary for the thermocouple in the chuck body (5) the thermocouple in the top plate (3) is an isolated type to eliminate possible electrical interferences. Both of the thermocouples each have two independent elements of type K sensitivity. Also seen in this view are the pipes (13) for the chuck vacuum supply (wafer hold) and the screws (14) which are used for locking and leveling the thermal chuck assembly.

c. The Automatic Wafer Prober

To build-in the capability for future automation of measurements, the thermal chuck assembly was adapted to a modified automatic wafer prober. This commercial prober has a probe ring assembly which can accommodate as many as sixty individually adjustable probes. Once mounted and adjusted, the probes remain fixed in space. Automatic probing is accomplished by moving the chuck-mounted wafer to the appropriate position relative to the probes. The prober provides a small vertical motion (z) to raise or lower the chuck in order to break or make contact between the wafer and the probes; x-y translation is then accomplished by a table to which the chuck is mounted. After reaching the new position, the z motion is actuated to make contact with the device. This automatic feature completely eliminates manual alignment of probes after the initial alignment. The probing machine is also able to index from die-to-die at a preset interval to allow automatic probing of identical devices at fixed intervals on the wafer.

d. Control of the Wafer Ambient

The low temperature requirements of the thermally stimulated measurements dictate the use of a cryogenic fluid for the thermal chuck coolant. The availability and the relatively non-hazardous nature of liquid nitrogen makes it ideally suited for these experiments. However, the low temperatures it provides impose rather stringent environmental conditions for the thermal chuck. The main problem is to maintain a relatively dry ambient to minimize or eliminate the condensation of water vapor on the wafer at low temperatures. For this reason, it is necessary to operate the chuck within a dry environment.

The required dry ambient was provided by enclosing the thermal chuck and the wafer prober in a hermetically sealed box. The enclosure is continuously purged ($\approx$2.5 sLpm) with dry nitrogen to minimize moisture penetration. The main features of the box are shown in the four views of figure 13 (refer to table 4 for the numerical listing of the components).

(a)

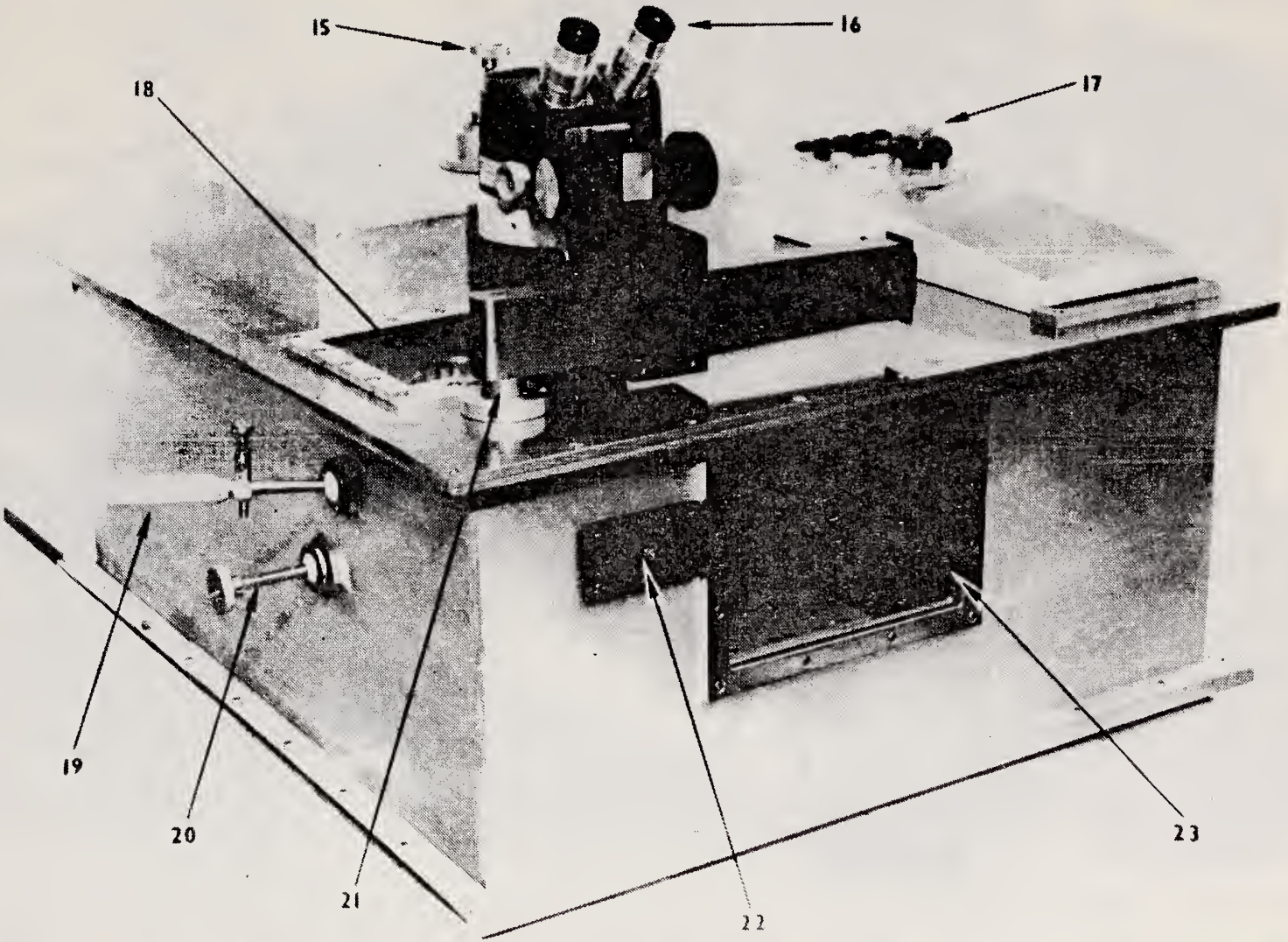


Figure 13. Four views of the wafer prober/thermal chuck system: (a) Front view. (The numbers indicate major components of the assembly listed in table 4.)

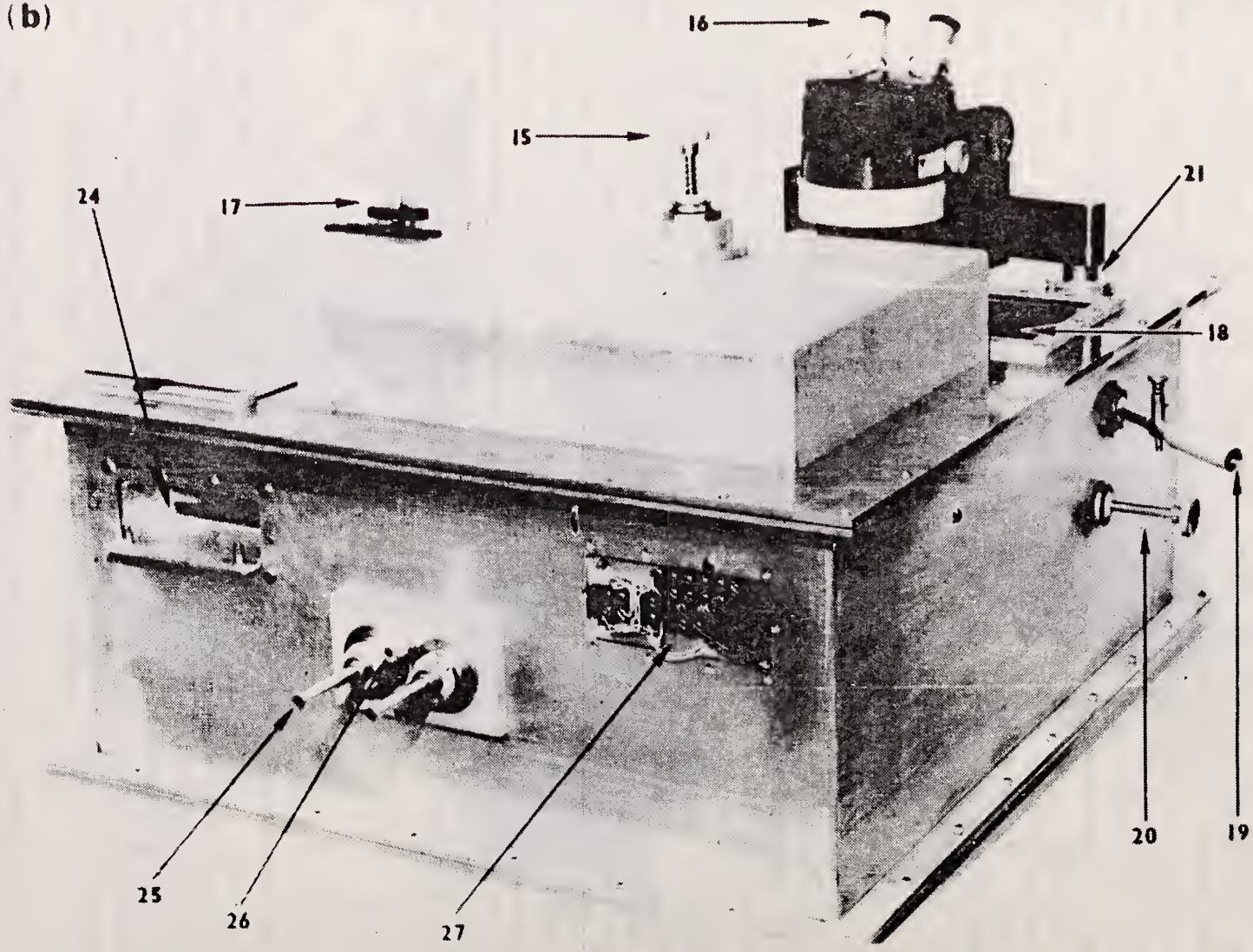


Figure 13. Four views of the wafer prober/thermal chuck system: (b) Back view. (The numbers indicate major components of the assembly listed in table 4.)

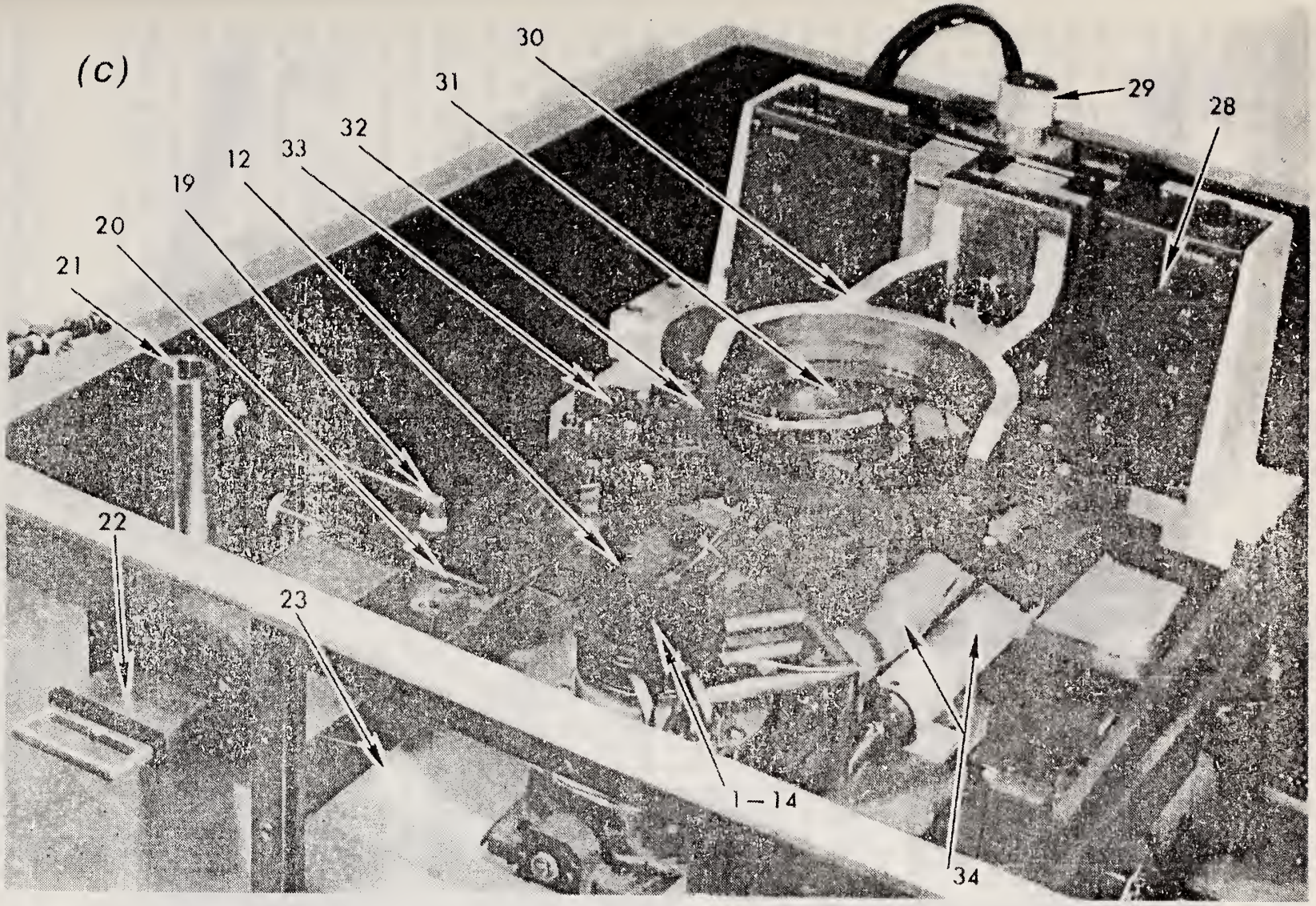


Figure 13. Four views of the wafer prober/thermal chuck system: (c) Inside view. (The numbers indicate major components of the assembly listed in table 4.)

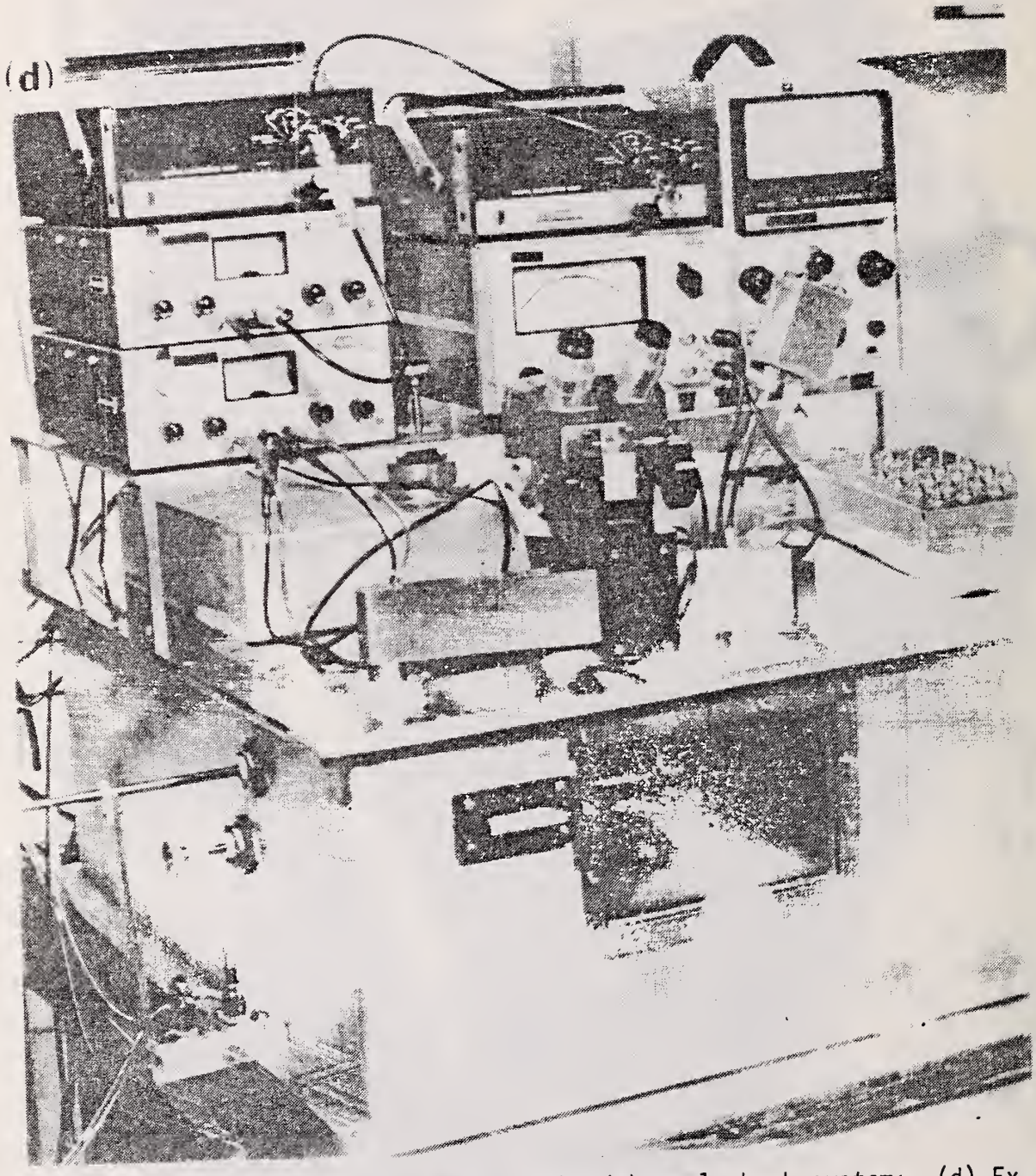


Figure 13. Four views of the wafer prober/thermal chuck system: (d) Experimental setup with instruments.

All sealing surfaces utilize gaskets or "O" rings. The front view (fig. 13a) shows the two view ports (18, 23), the prober control panel (17), and the microscope (16). Utilities are interfaced to the back of the box; these include the prober control (24), liquid nitrogen feed-throughs (25), dry nitrogen feed-throughs (26), heater power leads and thermocouples (27) (see fig. 13b). Figure 13c shows an inside view of the prober box. The thermal chuck assembly is seen in the foreground. In operation, a wafer is loaded into the box with the wafer transfer slide (22); once inside the box, the wafer is picked up with the vacuum-operated wafer transfer probe (19) and placed on the surface of the thermal chuck. Specimen wafers can be changed in a matter of seconds without having to open the box; the wafer slide assembly (22), which is sealed to the box in both the open and closed positions, minimizes room air penetration into the box. Wafer alignment to the prober axis is accomplished by rotating the chuck assembly with the θ-manipulator (20); this is done while viewing the wafer with the microscope (16) through the top viewport (18). The prober's bridge structure (28), which supports the probe ring (32), is shown displaced rearward for clarity; the probe ring is normally in the region above the thermal chuck. Mounted on the probe ring (32) are six individually adjustable probe manipulators (33), and a 6 by 6 multiprobe array (31); these are shown in greater detail in figure 14. The commercial manipulators were modified so that they could accept either the conventional probe tip (fig. 14a) or a coaxially shielded probe tip (fig. 14b). The multiprobe (fig. 14c) is a fixed array of 36 probes spaced at 5.08-mm intervals; it was designed specifically to simultaneously probe 36 MOS capacitors on a wafer for mobile ion measurements using the bias-temperature stress (BTS) test. The BTS is performed at 300°C with a stress field of 10^6 v/cm for 5 min; the mobile ion charge is determined from the net difference of the flat-band voltage shift as a result of positive and negative BTS. Each of the 36 probes is electrically accessible during BTS to allow removal of defective devices from the circuit. The relative spacings of neither the individual probes (33) nor the multiprobe array (31) can be adjusted after the box is closed. However, fine adjustment of the probe contact pressures is available with the height micrometer (29) which is accessible externally by the probe ring height manipulator (15). Also seen in figure 14c are the two telescoping tubes which enclose stainless steel bellows (34) to transport the liquid nitrogen to and from the thermal chuck. The telescoping tubes are necessary to mechanically confine the bellows to minimize motion caused by the gaseous expansion of the liquid nitrogen during a cooling cycle. The tubes also insulate the bellows from the ambient to minimize cooling of the dry nitrogen ambient. Under measurement conditions, the top and front viewports (18, 23) are covered to prevent light from entering the box. Figure 13d shows a view of the apparatus with its normal complement of instrumentation.

e. Apparatus Capabilities

The apparatus has been subjected to a series of tests to determine its functional performance. Table 5 lists the thermal capabilities of the

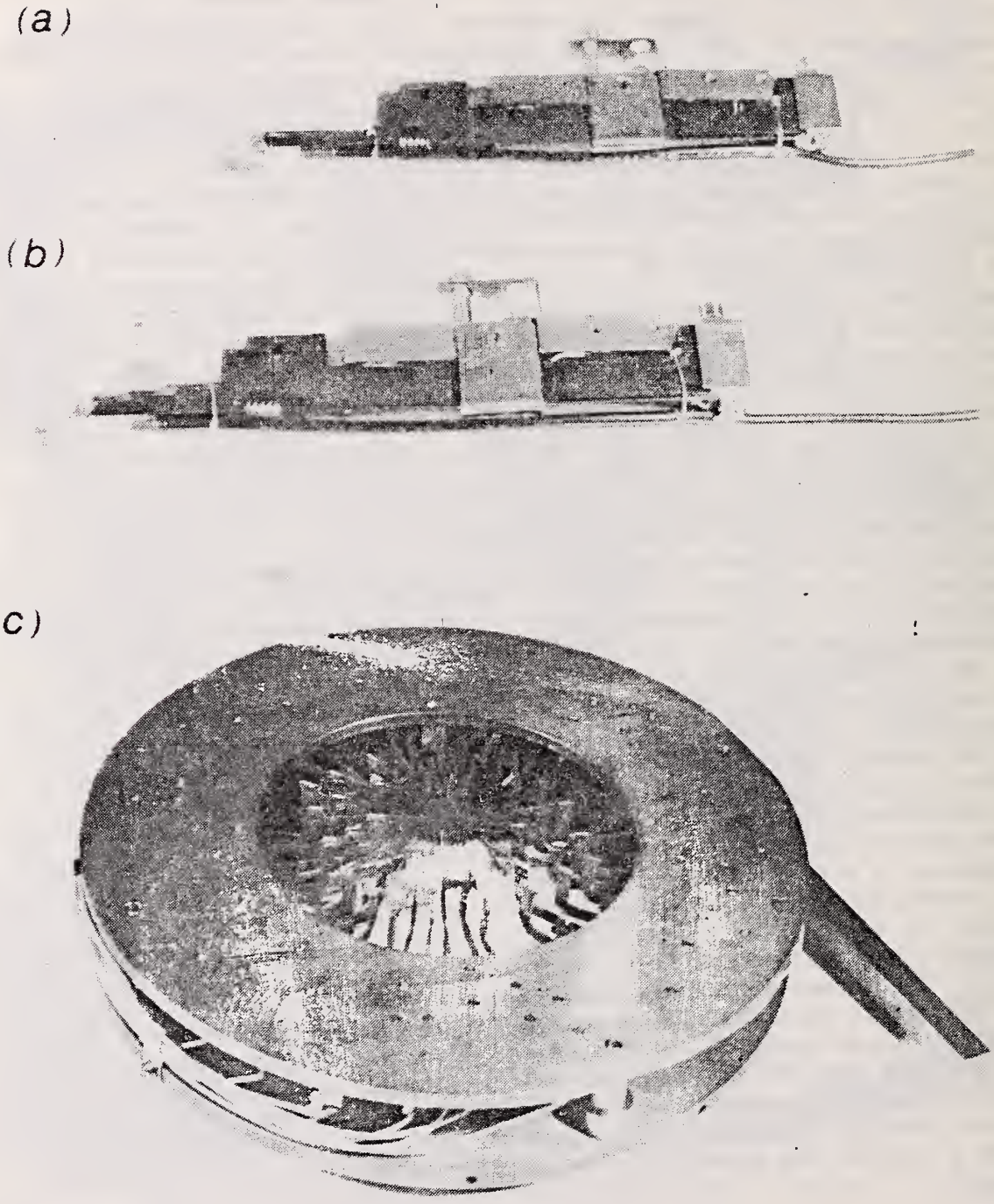


Figure 14. Detailed views of the available probes: (a) commercial manipulator with standard probe tip, (b) commercial manipulator with coaxial probe tip, and (c) 6 by 6 multiprobe array (inverted).

Table 5 — Performance Specifications of the Thermal Chuck

No.	Characteristic	
1	Low temperature limit of top surface	-194°C (79 K)
2	Low temperature limit of chuck body	-195°C (78 K)
3	Minimum high temperature limit	≈350°C (≈623 K)
4	Elapsed time from room temperature to low temperature limit	<4 min
5	Elapsed time from low temperature limit to room temperature	<45 s
6	Heating rate from low temperature limit to room temperature	>6.5 K/s
7	Elapsed time from room temperature to 300°C	<70 s
8	Elapsed time from 300°C to room temperature	<110 s

chuck that were measured; these capabilities easily satisfy the thermal attributes listed on table 3. The high heating rate at low temperature allows thermally stimulated current measurements to be made with favorable signal-to-noise ratios. The ability to reach temperatures below 80 K maximizes the energy range of detectable defects. The automatic features of the prober minimize the time required to adjust and align probes on the wafer. This makes feasible the testing of many devices on the same wafer for the purpose of wafer mapping. In addition, the high heating and cooling rate between room temperature and 300°C (along with the multiprobe) drastically reduces the time required for the BTS test. The system has been used to perform TSM in both the current and capacitance modes on both *pn* junctions and MOS capacitors. Currents as small as 200 fA (0.2 pA) and capacitance changes as small as 5 fF (0.005 pF) can be detected.

f. TSM and Wafer Mapping

Gold is frequently used to control the lifetime or the switching characteristic of high power diodes and thyristors. It is known to produce at least two centers in the band gap of silicon: an acceptor at E_c - 0.55 eV and a donor at E_v + 0.35 eV [15]. The gold centers are generally produced by diffusing the gold near the end of the wafer fabrication procedure. The uniformity of the electrical activity of such centers on wafer-sized power devices is an important consideration in the ability of the device to switch uniformly over its entire area. The measurements discussed in this section directly address the question of the uniformity of the electrical activity of the gold defect centers in silicon.

As a demonstration of its wafer mapping capability, the probing apparatus was used to map the gold donor concentration in a processed wafer. Thermally stimulated current and capacitance measurements were made on the 432-μm diameter base-collector gated diode (structure 3.10) of NBS-3 [12]. This test structure is repeated at 5.08-mm intervals; there are about 70 identical devices on a standard 2-in. diameter wafer. The thermally stimulated measurements (TSM) were repeated across the wafer at 5.08-mm intervals using the apparatus.

The n^+p gated diodes were fabricated by a typical bipolar procedure. After growth of the field oxide, the n^+ base regions were formed by diffusing phosphorus into <111>, 5-10 Ω·cm, *p*-type silicon (boron doped); the junctions were about 1.5 to 2.0 μm deep. Although an emitter diffusion was performed to complete other test structures, it was not of consequence for the test diode considered here. The gold center was introduced by the diffusion of gold (from a back side evaporation) at 825°C for 24 h.

Figure 15 shows the thermally stimulated response from a typical diode on the processed wafer. The upper curve is the capacitance response and the lower is the current response. In each case, the response was measured by first cooling the device to near liquid nitrogen tempera-

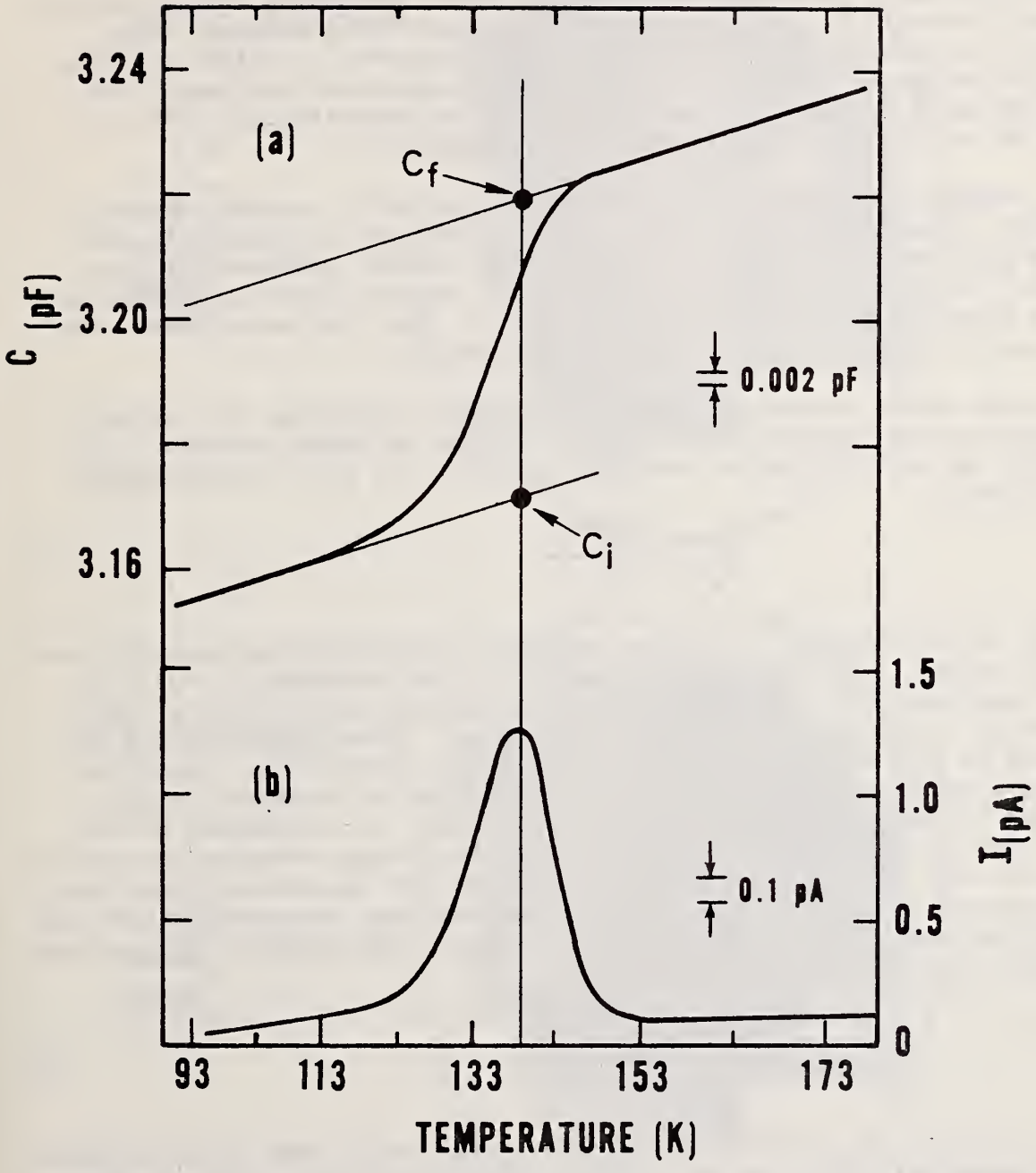


Figure 15. The thermally stimulated capacitance (a) and current (b) response of a gold-doped n^+p diode (heating rate ≈ 7 K/s).

ture. Zero bias was applied to the diode to charge all defects with majority carriers (holes); a reverse bias of 15 V was then applied to form a depletion region. The current or capacitance was measured with the depletion bias maintained while the wafer was heated with a heating rate of about 7 K/s. At the appropriate temperature the gold donor emits its trapped hole causing a measurable current, a slight collapse of the depletion region, and a measurable capacitance increase. The system noise in the x-y recorder tracings was approximately 2 fF and 100 fA for the capacitance and current respectively.

The thermally stimulated current response is useful in establishing a "quick" identification of a defect if its response is known. In this case gold was purposely introduced and the current response verifies this. The topic of interest, however, is the gold donor concentration as a function of the position on the wafer. For this measurement, the thermally stimulated capacitance is more useful.

The gold donor concentration was determined by measuring the thermally stimulated capacitance response as a function of wafer position. Following the work of Buehler and Phillips [10], the defect concentration is given by

$$\frac{N_t}{N_A} \simeq \frac{2(C_f - C_i)}{C_f} \tag{2}$$

N_t/N_A is the ratio of the defect density to the background acceptor density; C_f and C_i are given in figure 15a. This expression is valid for the case when only one charge carrier is emitted, and $C_b^2 >> C_i^2$ [10] where C_b is the zero bias diode capacitance. These conditions are satisfied in this measurement of the gold donor concentration. Note that in this measurement only the total charge flow, as evidenced by the change in capacitance, is important; the result is independent of the heating rate. An independent measure of the average acceptor concentration of the depletion region is required and was determined from a room temperature measurement of the capacitance-voltage characteristic of the same junction used for the TSM. The acceptor concentration, N_A, was calculated from the Schottky equation:

$$N_A = \frac{2C_1^2C_2^2(V_2 - V_1)}{qK_s\varepsilon_o(C_1^2 - C_2^2)} . \tag{3}$$

C_1, V_1 and C_2, V_2 are the capacitance-voltage pairs taken from the diode C-V characteristic; q is the electronic charge, K_s is the relative dielectric constant for silicon, and ε_o is the permittivity of free space. C_1 and C_2 were measured with applied reverse bias voltages of 5 and 15 volts, respectively, for V_1 and V_2. These data were used to calculate the absolute defect concentration from eq (2). Figure 16 displays the gold donor concentration (16a) and the boron acceptor concentration (16b)

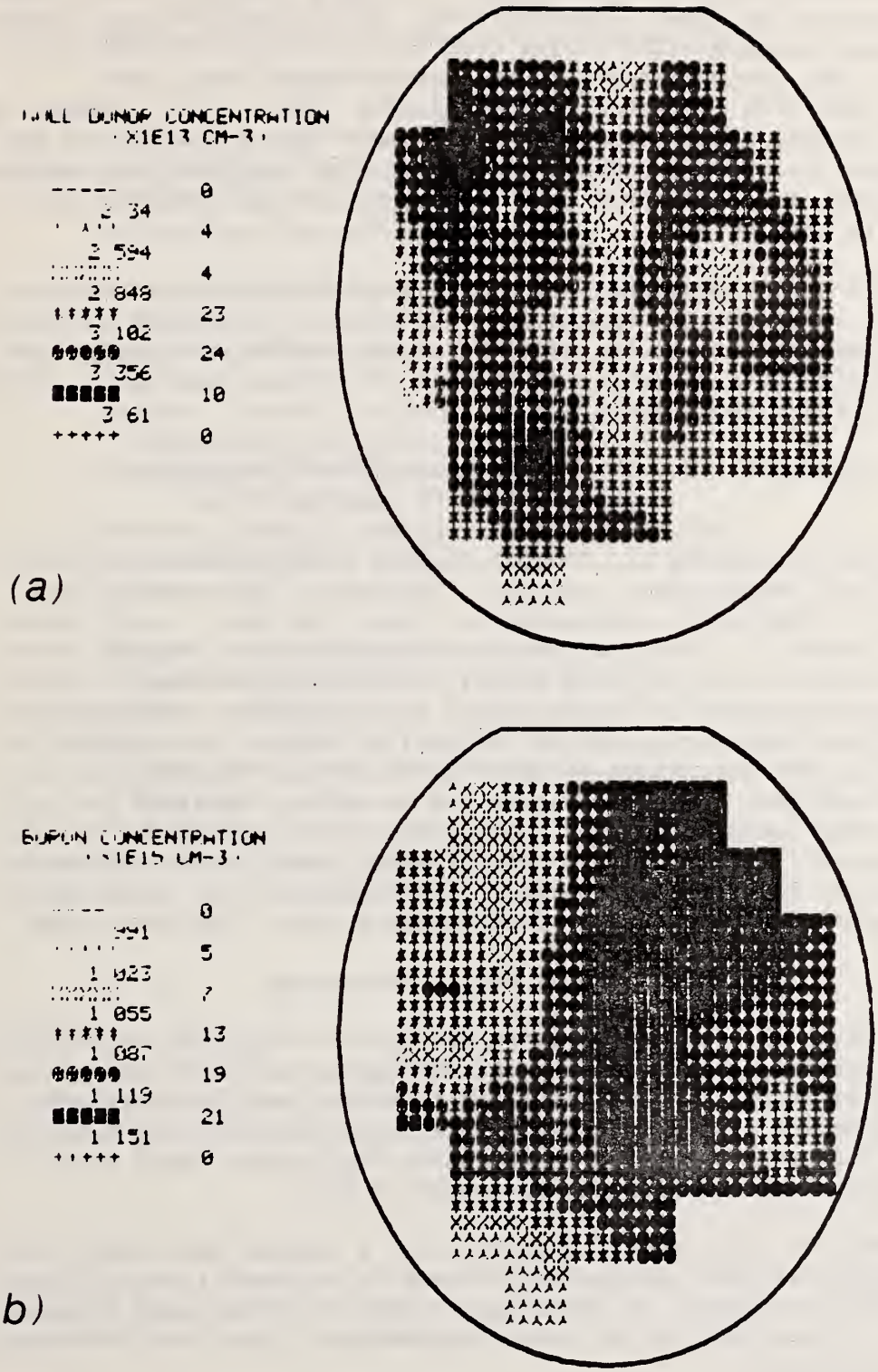


Figure 16. Wafer maps of (a) the gold donor concentration in the collector and (b) the collector boron acceptor concentration.

as a function of position on the wafer.† In each case the darker areas represent regions of higher concentration. As indicated on the figures, the gold donor concentration varies from 2.34 to 3.61 × $10^{13}/cm^3$ (54% variation). The boron acceptor concentration ranges from 1.0 to 1.15 × $10^{15}/cm^3$ (15% variation). Judging from figure 16, it appears that there is no relationship between the gold donor defect density and the boron acceptor background. The system noise (2 fF or 0.002 pF) suggests that gold donor concentrations in the range of 1 × 10^{12} cm^{-3} would be detectable in this wafer.

These results demonstrate the unique capabilities of this temperature controllable wafer probing apparatus. The ability to perform thermally stimulated measurements at the wafer level for process control or process diagnostics is a valuable addition to the process engineer's selection of analytical tools.

3.5 Objective 1.3: The Feasibility of Utilizing TSM at Intermediate Processing Points

Typical device processing for the fabrication of high power thyristors includes a high temperature, long term diffusion. This results in a wafer which is completely surrounded by a deep junction: a *pnp* structure. As a result of this process, the lifetime of the original material is reduced as much as three orders of magnitude because of the introduction or activation of electrically active defects. The specific reason for this degradation and the ability to monitor the presence of defects during the processing of material would be a valuable aid to the process engineer and could assist him in making decisions for further processing based on current knowledge of the state of the material. Since TSM could directly address this problem, power device processing procedures were investigated to assess the feasibility of using TSM on processed power device wafers by fabricating special test structures.

a. Basic Power Device Processing

A study of basic thyristor processing was made to determine at what intermediate steps in the processing the TSM techniques could be applied. To aid in this study, a number of major thyristor manufacturers were visited; these are listed in table 6. Although the different manufacturers use different processes to fabricate thyristors, there is a "basic" process which appears to be common to all.

Table 7 lists the basic processing steps for a typical high power thyristor. The first high temperature process is a closed tube diffusion (see fig. 17; the numbers in parentheses refer to the process sequence of table 7). This step (3) is a high temperature, long term diffusion

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†There are actually about 70 data points plotted on a grid corresponding to the 5.08-mm interval of the devices on the wafer. For display purposes there are three intermediate points between each pair of actual data points, whose shading is derived by interpolation.

Table 6 — A List of the Various Power Semiconductor Facilities Visited During 1976

Company
Westinghouse Electric Corp., Research and Development Center, Pittsburgh, Pennsylvania
Westinghouse Electric Corp., Semiconductor Division, Youngwood, Pennsylvania
General Electric Company, Static Power Conversion Operation, Collingdale, Pennsylvania
General Electric Company, Corporate Research and Development Laboratories Schenectady, New York
General Electric Company, Semiconductor Products Department Auburn, New York
International Rectifier, Semiconductor Division, El Segundo, California

Table 7 — Basic Thyristor Processing Steps

(1) Wafer preparation (saw, lap)

(2) Chemical cleanup

(3) Single or multiple closed tube, high temperature (≈1250°C), long term (12-72 hrs.) diffusions (p-layer)

(4) Open tube emitter diffusion (n-layer) (≈1100-1200°C)

(5) Lifetime control by impurity diffusion

(6) Backing plate (≈800°C)

(7) Top side metal masking

(8) Edge contouring and junction passivation

(9) Lifetime control by e-radiation

(10) Packaging

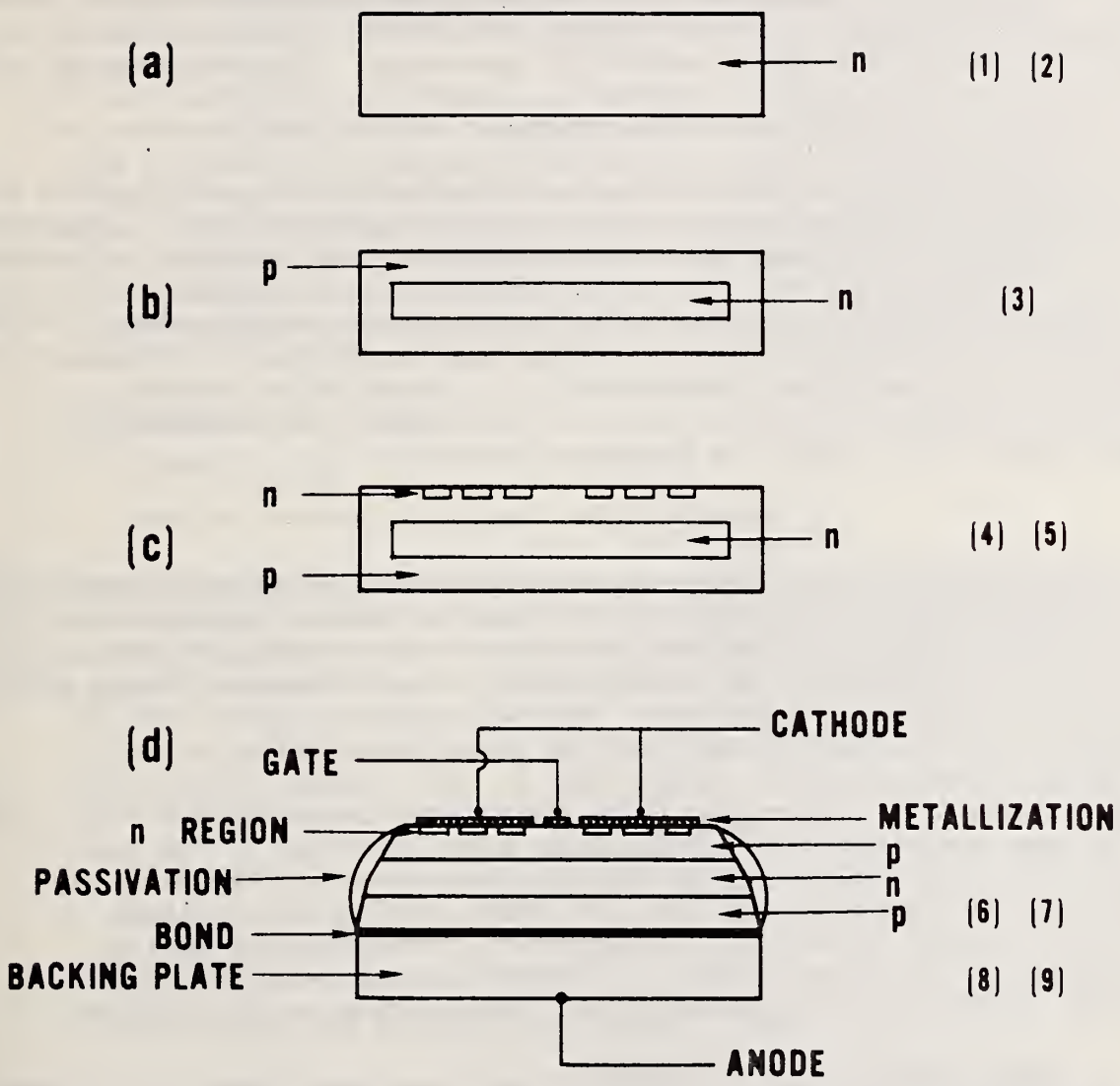

Figure 17. Schematic of basic thyristor processing. The numbers in parentheses refer to the process outline of table 7.

to form the deep junctions bounding the *n*-region. At this stage, a *pnp* structure is formed, but the two junctions are shorted at the edge (fig. 17b). The time for the *p*-diffusion determines the final thickness of the interior *n*-region; this thickness, along with the dopant density determines the reverse blocking characteristics of the device. The next major processing step is the emitter diffusion (step 4, fig. 17c). This is an open tube *n*-type diffusion to form the cathode region of the thyristor. The cathode configuration is defined photolithographically. At this point some form of lifetime control treatment (step 5) is used to "tailor" the switching characteristic of the device. The tailoring can be completed at this stage or carried to a point in preparation for final adjustment to be done at a later stage in step 9. The processed wafer is then bonded to a metal backing plate (step 6) for rigidity and ease of handling in the packaging steps. After metallization (step 7) for the gate and cathode (transmission mask or photolithographic operation), the edge of the wafer and the backing plate are contoured to isolate the junction (step 8). This step removes the *p*-skin which was shorting the *n*-layer at the edge. The junction edge is appropriately passivated to withstand the rated reverse blocking voltage. If further tailoring of the switching characteristic is prescribed or required, electron irradiation can be utilized at this point. The completed thyristor wafer is then ready for packaging (step 10).

b. Possible Test Structures

For this thyristor process, the most interesting and meaningful evaluations should be made after steps 2, 3, 4, and 5. TSM is feasible at any of these points, provided that appropriate test structures (MOS capacitors or *pn* junctions) can be fabricated so that electrical contact to regions of interest is possible. The MOS capacitor formed with low temperature processing (see sec. 3.3) is suited for starting material evaluation (steps 1 and 2). Beyond step 3, the *n*-region, which is of primary interest in this study, is no longer directly accessible. A special test structure is required, which takes advantage of the existing diffused *pn* junction. An isolated *pn* junction for the study of the *n*-region is the obvious structure. The basic problem is as follows: given the wafer as illustrated in figure 17b, isolate one or more *pn* junctions which would be suitable for thermally stimulated measurements. There are several attributes required of the solution to this problem:

1. make contact to the *p*-region,
2. make contact to the *n*-region,
3. define and isolate the *pn* junction diode,
4. passivate the junction so that leakage currents are acceptably small,
5. use processing techniques which do not alter the properties of the region of interest, and
6. make measurements in wafer form.

Without being specific about the details of processing at this point, the diodes illustrated in figure 18 are two configurations which may be appropriate for the junction test vehicle. In either case, a number of mesa diodes would be fabricated by chemical or physical etching, mechanical sawing, or a combination of techniques. One possible form of passivation would be chemical vapor deposited silicon dioxide (CVD-SiO_2). Figure 18a shows a cross section of a single diode on the wafer with a top side *n*-region contact. In figure 18b, the back side has been lapped to remove the *p*-region and metallized for a large area *n*-type contact.

3.6 Objective 2.1: Test Structure Development

The study of the process details for power device fabrication, and the conceptual design of the possible test structures provided the background for designing and fabricating test structures on the diffused power device wafers which would be suitable for use with the TSM technique. Three separate approaches were considered for the formation of the mesa diode structure. These were:

1. ultrasonic machining
2. plasma etching
3. chemical etching

Using existing mask sets (NBS-2 [16] and a dot matrix), mesa diodes were fabricated using the ultrasonic machining and plasma etching techniques. Initial results indicate that either the ultrasonic machining or the plasma etching technique can be used to make diodes for TSM.

a. Ultrasonically Machined Mesa Diodes

The ultrasonic technique involves the following steps:

1. ultrasonically machine the moat to form the mesa
2. chemical cleanup
3. passivation
4. contact cut and metallization (NBS-2 [16])

A special ultrasonic tool head was fabricated to allow the simultaneous formation of 22 mesas over the central region of a wafer. The wafer was protected by a thin (≈850-μm) glass coverplate to prevent chipping during the ultrasonic procedure. About ten minutes was required to machine through the coverplate and approximately 75 μm into the silicon surface. The moat surrounding each mesa was briefly chemically etched to relieve the work damage. Chemical vapor deposition (CVD) of SiO_2 was used to passivate the junction which is exposed by the formation of the mesa. Contacts were made to the top side (*p*-diffusion) of the mesa and to the back side (*n*-region) of the wafer. Figure 19 shows a photograph of an ultrasonically formed mesa diode structure. The diode is about

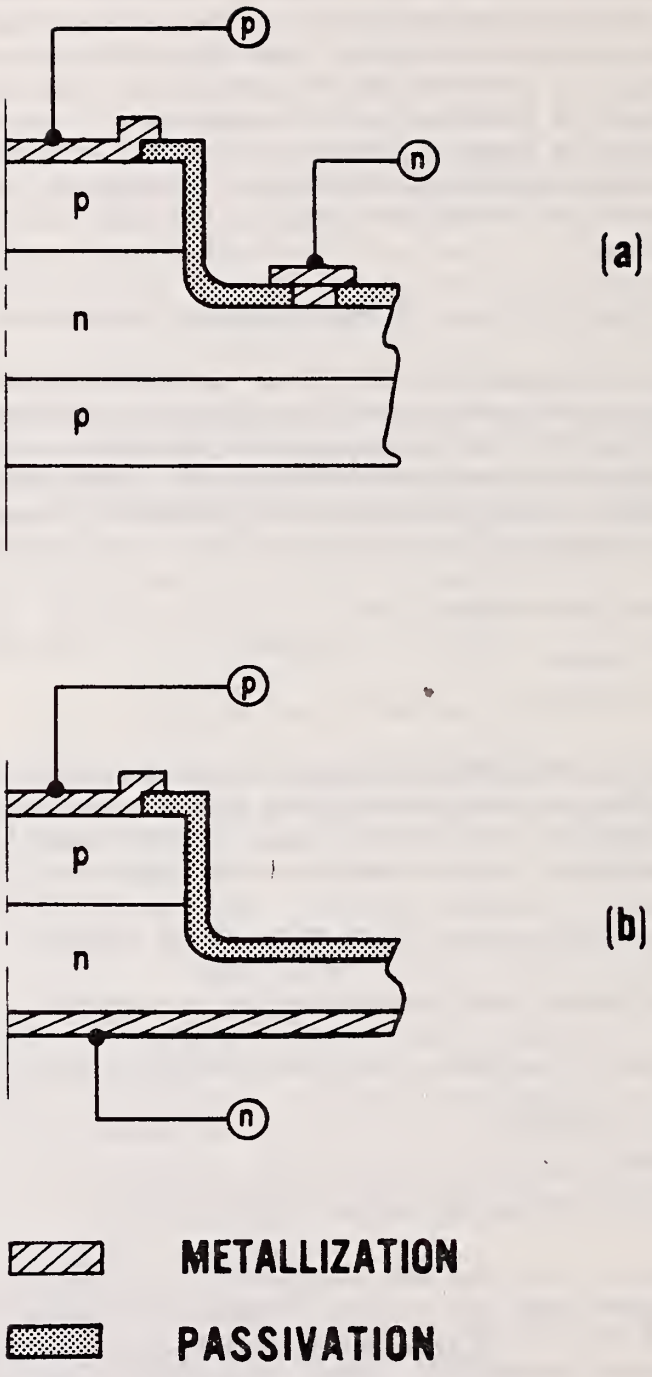

Figure 18. Cross sections of the proposed mesa diodes: (a) top side n-contact, (b) back side n-contact.

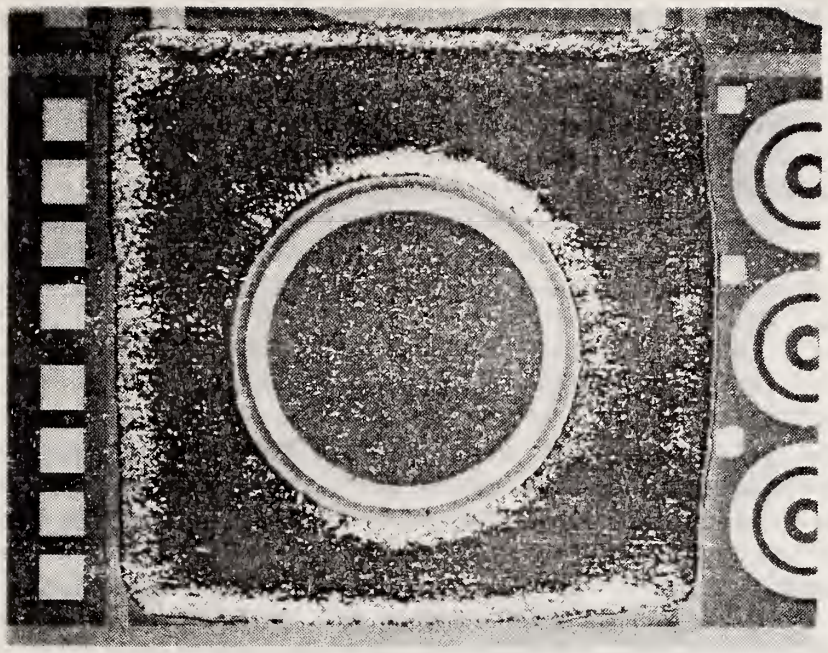

Figure 19. Photograph of the ultrasonically etched mesa diode; the major diameter of the mesa is about 1.5 mm.

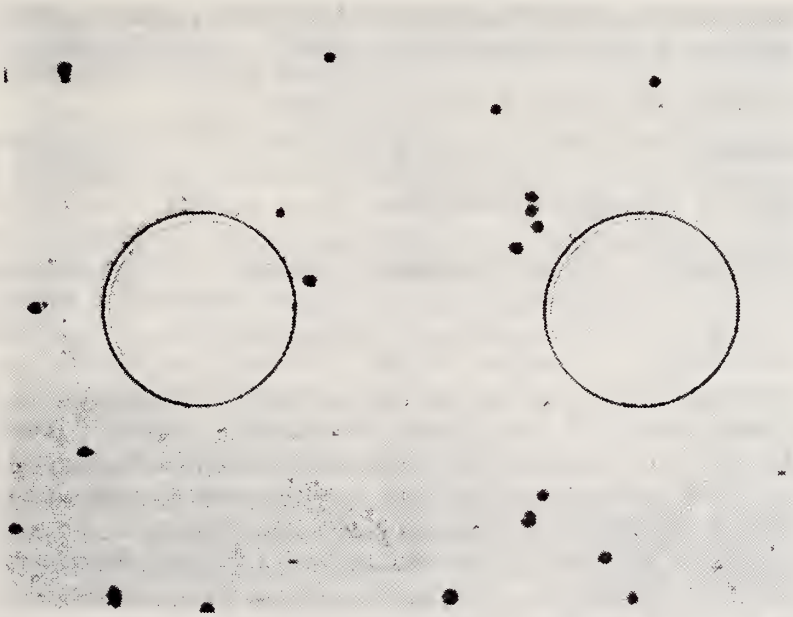

Figure 20. Photograph of the plasma etched mesa diode; the major diameter of the mesa is about 230 μm.

1.5 mm in diameter and the mesa is about 75 μm high; the top side contact is in the form of a ring (levels 3 and 4 of NBS-2 [16] were used to define the contact and metallization). Although the yield of devices was low, some 20 percent of the devices fabricated on several wafers had an acceptable reverse leakage current in the range of 10 nA at room temperature with an applied reverse bias of 10 volts. A majority of devices had leakage much higher than this; surface leakage is the probable source. The design of the special mask set will also include a gated structure to control surface leakage. The procedure for the ultrasonic fabrication of mesa diodes needs to be refined for reproducibility of device quality.

b. Plasma Etched Mesa Diodes

Plasma etching [17] is a "dry" chemical process which is used for removal of various materials in the semiconductor industry. In its present application, it is used to remove regions of silicon from the surface of the wafer not protected by the mesa mask. The RF plasma is used to excite an atmosphere of CF_4 and O_2 to produce various chemically reactive atoms, ions, electrons, and free radicals. These species chemically react with the surface to effectively etch the silicon.

The plasma etch technique for the formation of mesa diodes involved the following steps:

1. deposit mask material and photolithographically define mesa areas
2. plasma etch the moat to form the mesa
3. passivation
4. contact cut and metallization

Whereas the ultrasonically formed mesa is defined by the mechanical dimension of the tool, the plasma etch technique requires a mask to protect the mesa region while the moat is being etched. In a first attempt at using this technique, a thermal oxide (300 nm) was grown on a diffused wafer. The oxide was patterned by a photolithographic operation to protect the mesa areas of the diode structure. After plasma etching the moat, a thin (≈50-nm) oxide was thermally grown for the passivation. Finally, contact cuts were made and the contact metal was applied and patterned (a simple 3-level dot-matrix mask set was used for this fabrication procedure). The resulting structure (230-μm diameter) is shown in the photograph of figure 20. This procedure was successful in fabricating diodes of good leakage characteristics. Of the devices tested (>20) most had reverse leakage in the range of a few nanoamperes at room temperature with a 10-volt reverse bias. This is very suitable for TSM.

Although the plasma etched mesa in its current form is a definite possibility with respect to mesa diode fabrication, it has some disadvantages with respect to characterization of in-process power device material. One disadvantage is the relatively time-consuming step of the mesa

etch itself; it requires about twenty minutes to etch a few micrometers. This would be suitable for the analysis of diffused solar cell material or for devices with shallow junctions. However, for power device material, where junction depths could be as deep as 100 μm, it would be too time consuming. (This is a characteristic of current capabilities at NBS-ETD and is not necessarily true of all plasma etching machines; a machine with a higher etching rate may allow this technique to be useful for power device material as well.)

A more serious objection to the current plasma etch procedure is the thermal oxidation steps for the mask and passivation layers. There is the risk that these high temperature (≈1000°C) steps could alter the properties of the defects that we hope to study. The deep diffusion for power devices is usually done at temperatures in the range of 1200 to 1250°C for times ranging from 12 to 72 hours. Hence, a 1000°C oxidation for 20 min may be of no consequence; however, this remains an open question. If it can be shown that thermal oxidation does not alter the defect properties, then its use in masking and passivation would be acceptable for mesa diode fabrication (note that this is independent of the method used to form the mesa). Further studies will be made along these lines.

c. Chemically Etched Mesa Diodes

Due to anticipated severe undercutting, the chemical etching technique has not yet been implemented. Special procedures and a special mask set will be developed for this purpose.

The studies completed to date on this phase of the work have shown the feasibility of fabricating mesa diodes with low leakage characteristics for the TSM technique. Future work includes refinement of the processing procedures in order to allow reproducible fabrication of devices. In addition, the design of a special mask set to be used with mesa fabrication is planned, and will allow process variations to be evaluated so that an optimized mesa fabrication procedure can be specified.

3.7 Objective 2.2: Measurement Procedures

The utility of thermally stimulated measurements lies in their ability to 1) detect the presence of defects and 2) identify the particular defect. The ability to detect defects depends on being able to uniquely attribute a thermally stimulated current or capacitance response to a bulk defect, as opposed to a response caused by environmental or intrinsic interferences. The identification aspect relies on the existence of a "defect catalog" which details the response of specific known defects to thermal stimulation conditions. The goals of this objective are 1) to examine various interferences which could mask or distort the bulk defect response and 2) to develop measurement procedures to identify and catalog defects characteristic of processed power device material. Several interferences have been observed; specific analysis of defects in processed wafers awaits finalization of the mesa diode fabrication

procedures. A preliminary catalog of defects and heavy metal contaminants in silicon has been developed from the literature in another part of the Semiconductor Technology Program.

a. Interferences

During the course of experimental measurements on MOS capacitors and *pn* junctions on a large number of processed wafers, several different types of interferences have been observed. These interferences can be classified into two categories according to their origin: 1) environmental and 2) intrinsic. If severe, either type can obliterate the TSM scan. If the interference is subtle, it can add "new structure" to the TSM spectrum and allow possible misinterpretation. In order to fully utilize TSM, a knowledge and awareness of such interferences is required.

Common environmental interferences are caused by light, excess water vapor, and relative mechanical motion of the probe with respect to the device. The presence of light on the specimen can interfere with both the charge state of the defect or the equilibrium nature of the depletion region due to excess carriers. Hence, TSM, as discussed in this report, should be performed in the dark. Excess water vapor in the wafer ambient allows condensation when the wafer temperature is low. This generally leads to non-reproducible surface leakage currents much greater than the desired response. Dry ambients eliminate this problem. Although design of thermal chucks consider expansion and contraction due to thermal cycling, it is generally not possible to eliminate chuck motion completely. Relative motion between the probe and the wafer chuck can cause probe slippage or intermittent contact. This results in noise in the measurement; however, flexible probes and "soft" metallization (e.g., aluminum) have been used to alleviate the problem.

Observed interferences of origin intrinsic to the device include extraneous emission from trapped interfacial oxide charge or signals arising from the movement of mobile ions. The presence of mobile ions in MOS capacitors or gates of gated diodes could distort TSM spectra. An example of this effect is shown in figure 21. This particular MOS capacitor was fabricated by diffusing gold into an *n*-type thermally oxidized silicon wafer. The presence of mobile ions (from an undetermined source) in this wafer was determined by bias-temperature stress measurements. In general, repeated TSM scans on a given device were non-reproducible. However, by appropriately "conditioning" the capacitor, reproducible results were possible. Shown in figure 21 are three TSM responses of the same device under different conditions. Curve (a) is the TSM response of the as-processed MOS capacitor. There is a peak near the point where the phase I emission [10] of the gold acceptor occurs (arrow near 220 K): however, it is not clear that this is the phase I response of the acceptor. The phase II [10] response is seen to be very different from the normal response. The traditional response of the gold acceptor is shown by curve (b); it displays the phase I shoulder (225 K) and the phase II peak (280 K). This response was obtained by performing a BT stress on the capacitor to drive the mobile ions to the metal

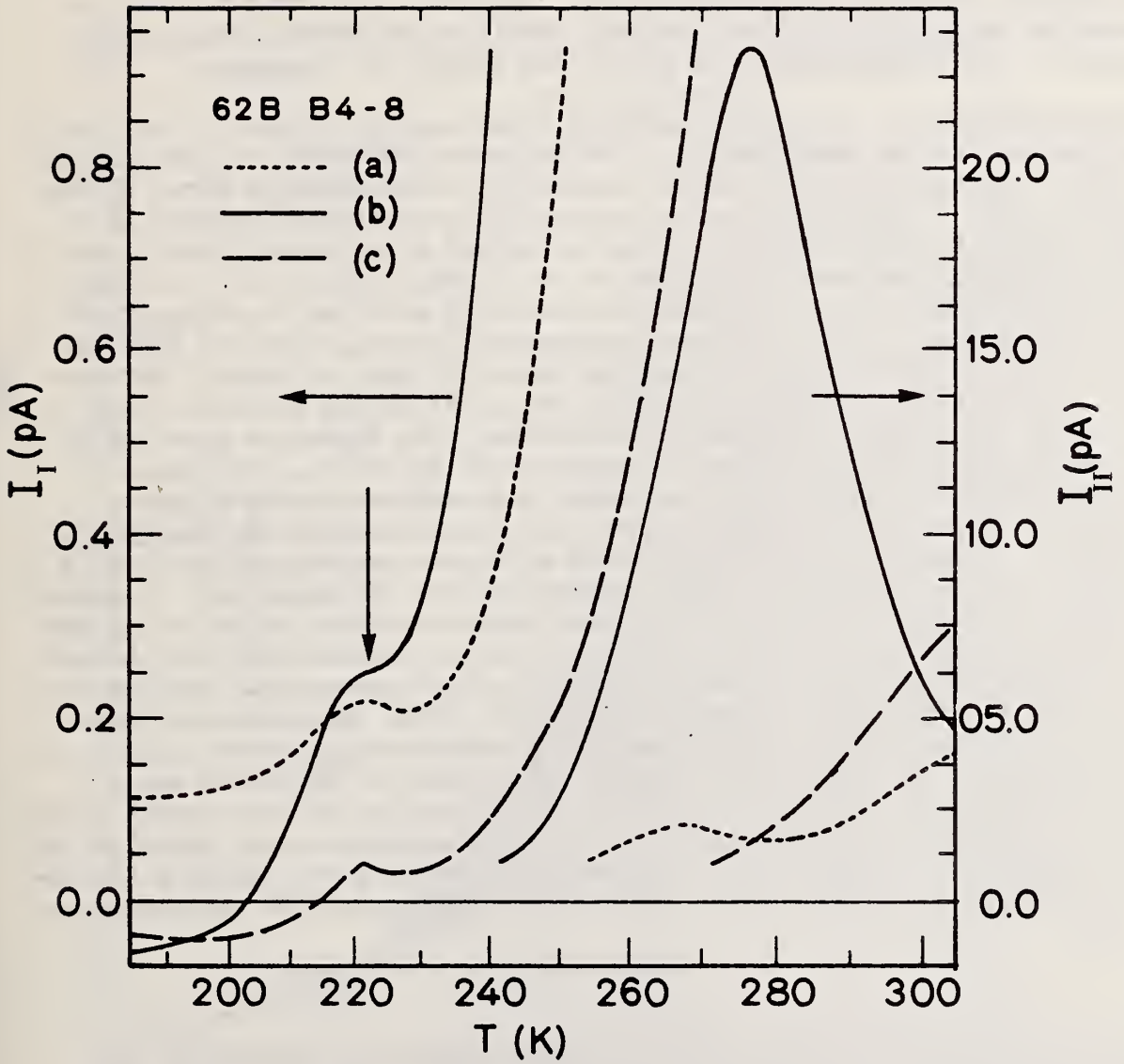

Figure 21. TSM response of an MOS capacitor contaminated by mobile ions: (a) as-processed device, (b) after moving the ions to the metal plate, and (c) after moving the ions to the Si-SiO_2 interface (heating rate ≈ 2 K/s).

electrode and is exactly the same as the response from an uncontaminated device. Curve (c) was obtained after BT stressing to drive the ions to the $Si-SiO_2$ interface. Again, there is a questionable phase I response and a very different phase II response. It appears from these measurements that the presence of mobile charge at or near the interface greatly affects the charge state or the emission process of the traps in the depletion region of the semiconductor. However, it is evident that by removing such mobile charge from the interface (by moving them to the metal) it is still possible to obtain the proper TSM response.

Although thermally stimulated emission from interface states is not well understood, it has been observed. These states can exist at the silicon-silicon dioxide interface of MOS capacitors or the gates of gated diodes used in TSM. Figure 22 shows the results of measurements made on an *n*-MOS capacitor with interface states introduced by electron irradiation.† The MOS capacitors were fabricated by dry thermal oxidation. The inset shows the measured C-V characteristic compared with the theoretically calculated curve [13]. The room temperature charging bias was fixed at -3 V (V_{b1}) in the interface distorted region of the C-V curve. TSM current response curves which resulted from six different depletion bias voltages (V_{b2}) at low temperature are shown. The structure near 243 K is believed to originate from interface state emission. The rather limited range in temperature over which the emission occurs suggests that the states are localized rather than distributed in the band gap of silicon. The large peak that develops at higher depletion bias (e.g., V_{b2} = -6 V) is the phase II [10] response of the MOS capacitor. A second example is shown in figure 23. In the current response of an *n*-type MOS capacitor fabricated as part of a bipolar wafer process with wet thermal oxidation, the emission is seen to begin at low temperatures and continues with no features to higher temperatures. This characteristic suggests that the emission originates from a continuum of states located in the band gap. If improperly treated, either type of interface state emission (fig. 22 or 23) could reduce the visibility of bulk defect emission. However, it is important to note that interface state emission, in most cases, can be shut off by appropriately setting the charging and depletion bias voltages to effectively prevent emission from the interface state.

b. Defect Analysis

Specific analysis of defects in processed power device wafers has not yet been started. This awaits the fabrication of mesa diodes and the establishment of appropriate measurement procedures. The objective is to measure the energy level and emission coefficient for defects in diffused power device wafers and catalog this data in a form useful for defect identification by TSM. An example of such a catalog for some metallic impurity and radiation induced defects in *n*-type silicon is shown in figure 24 [18]. Plotted is the heating rate dependence of the emission

†The irradiation at 1.5 MeV to a dose of 2.85×10^{14} cm^{-2} was provided by E. Sun of General Electric, Auburn, NY.

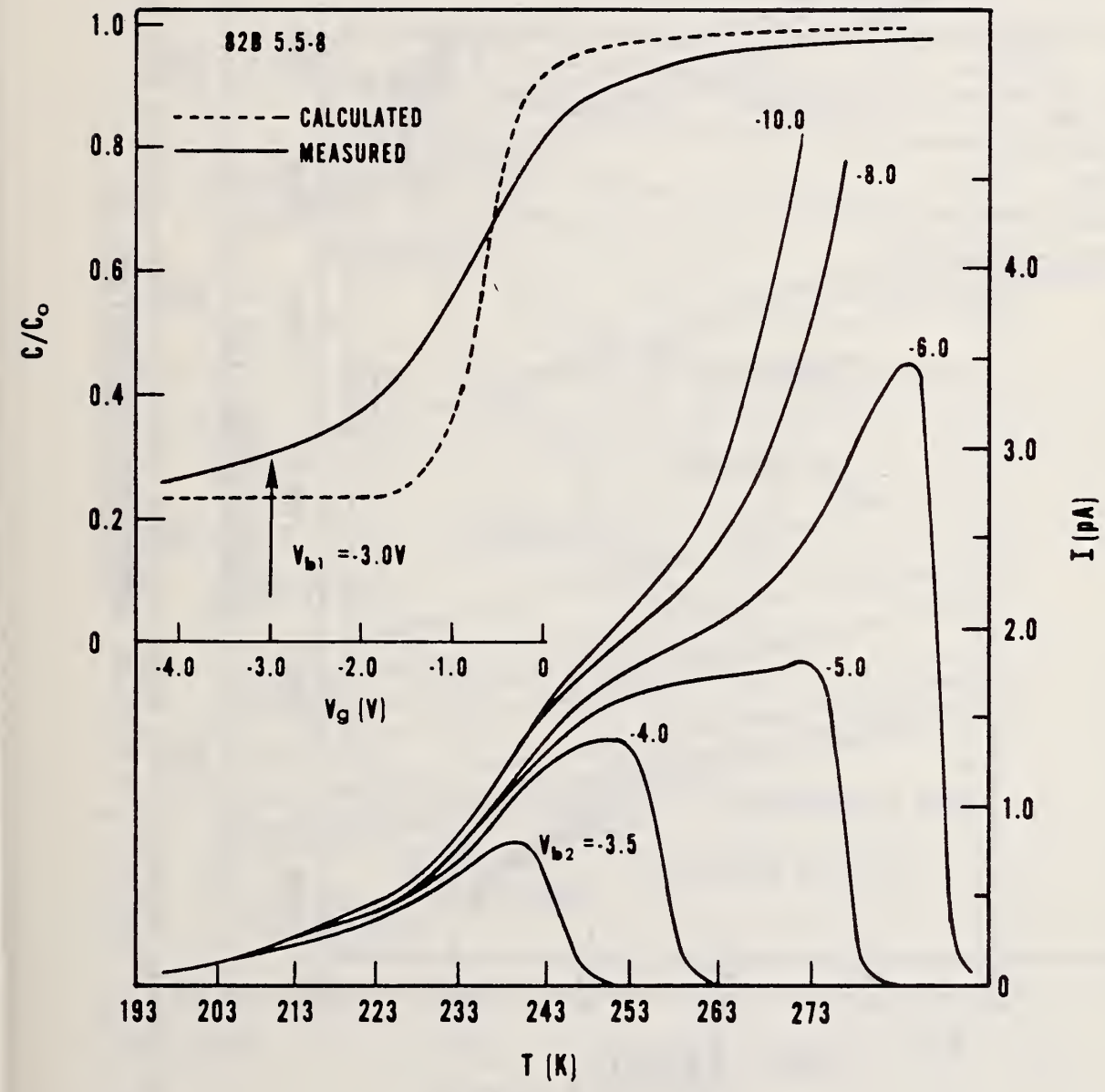

Figure 22. TSM current response of an electron irradiated n-MOS capacitor (1.5 MeV, 2.85 × 10^{14} cm^{-2}), with depletion bias as the parameter. The inset shows the measured C-V curve compared to the theoretically calculated one. (C_o = 34.6 pF, X_o = 0.114 μm, heating rate ≈ 7 K/s)

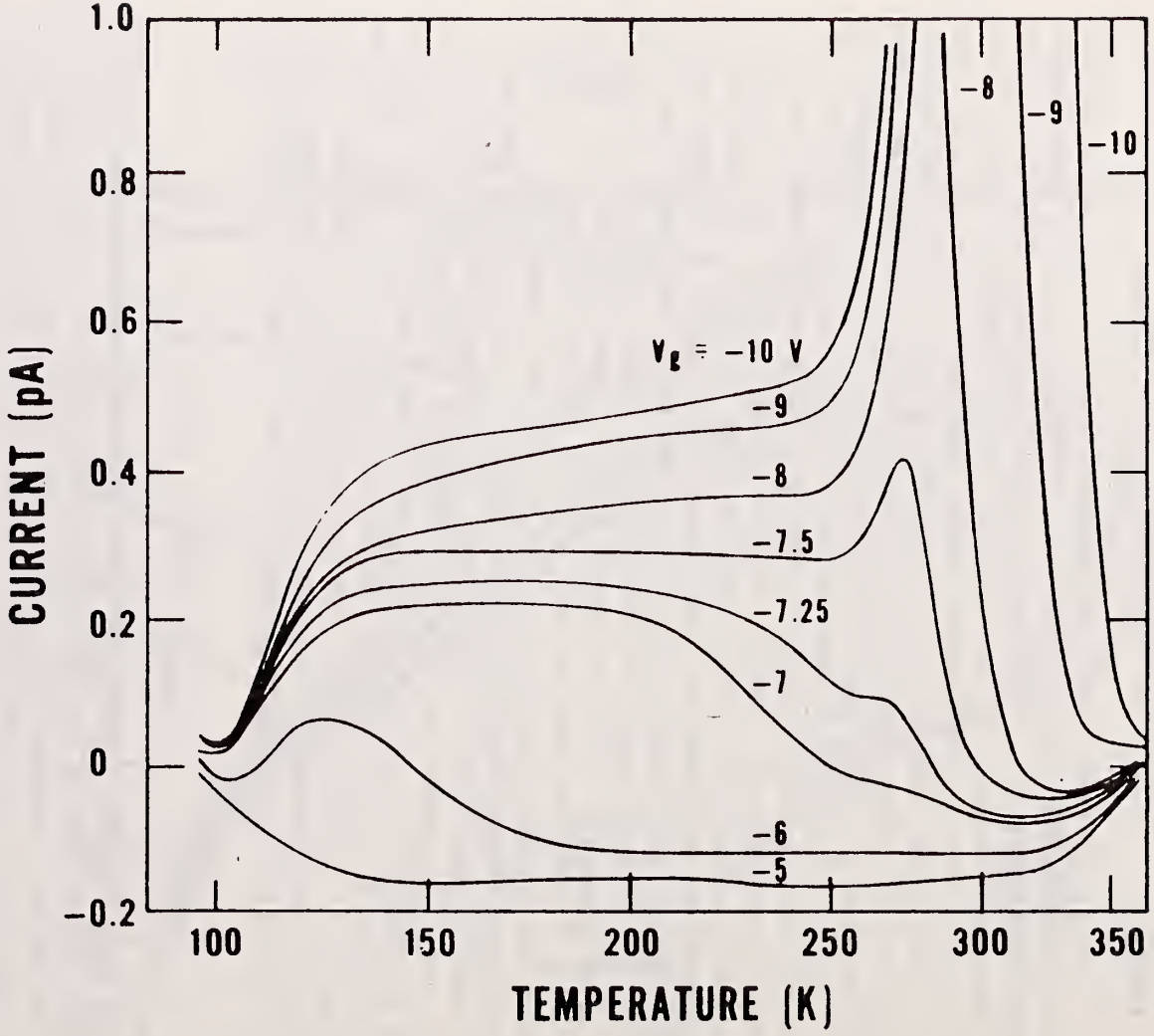

Figure 23. TSM current response of an n-MOS capacitor fabricated with wet oxide with depletion bias as the parameter. (C_o = 10.0 pF, X_o = 0.39 μm, heating rate ≈ 10 K/s)

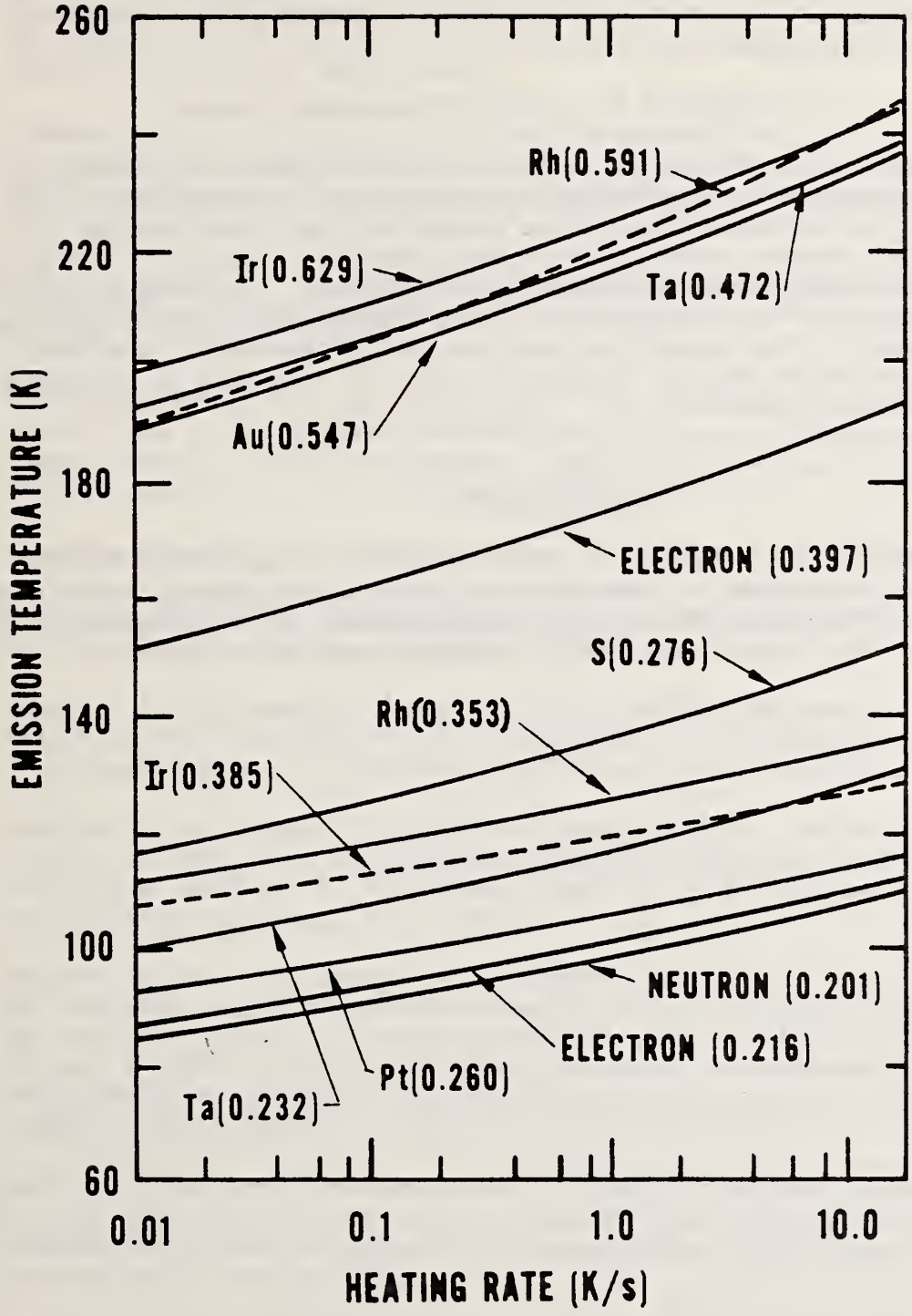

Figure 24. A tentative defect catalog for n-type silicon to be used with TSM experiments (energy levels are shown in parentheses [17]).

peak temperature; the associated energy level is shown in parentheses. Identification of a specific defect consists of measuring the TSM current response (at a known heating rate) and comparing it to known defects on the catalog.

3.8 Objective 2.3: Other Measurement Methods

The effort under this objective will be aimed at the establishment of two other measurement capabilities related to the TSM technique. The first is the transient capacitance method for deep level studies [19]. This method appears promising as a complementary technique to TSM for measuring energy levels and emission coefficients. The second objective is to determine the feasibility of using TSM for depth profiling of defect centers. This capability adds the third dimension to the two-dimensional wafer mapping capability. Work in this area is scheduled to begin in April, 1977.

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18. The following sources were used for the calculated data of figure 24:

Neutron (0.201), Electron (0.216), Electron (0.397)

Buehler, M. G., Investigation of Radiation-Induced Defects in Silicon *P-N* Junctions, AFCRL-72-0578 (September 1, 1972).

Iridium (0.385), Iridium (0.629), Rhodium (0.353), Rhodium (0.591)

Lisiak, K. P., and Milnes, A. G., Rhodium and Iridium as Deep Impurities in Silicon, *Solid-State Electronics* 19, 115-119 (1976).

Tantalum (0.232), Tantalum (0.472)

Miyata, K., and Sah, C. T., Thermal Emission Rates and Activation Energies of Electrons at Tantalum Centers in Silicon, *Solid-State Electronics* 19, 611-613 (1976).

Platinum (0.260)

Miller, M. D., Schade, H., and Nuese, C. J., Use of Platinum for Lifetime Control in Power Devices, *Technical Digest*, 1975 International Electron Devices Meeting, Washington, D.C., December 1-3, 1975, pp. 180-183.

Sulfur (0.276)

Rosier, L. L., and Sah, C. T., Thermal Emission and Capture of Electrons at Sulfur Centers in Silicon, *Solid-State Electronics* 14, 41-54 (1971).

Gold (0.547)

Sah, C. T., Forbes, L., Rosier, L. L., Tasch, A. F., Jr., and Tole, A. B., Thermal Emission Rates of Carriers at Gold Centers in Silicon, *Appl. Phys. Letters* 15, 145-148 (1969).

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APPENDIX A

TYPICAL CALCULATOR/CONTROLLER PROGRAM

for measuring, recording, and plotting the data needed to determine the resistivity of a silicon wafer by the photovoltaic method.

```
0: dim A$[1],B$[1],C$[8],D$[4],E$[12],F$[1]
1: ent "Calibrate? (Y/N)",A$
2: if A$="Y";gsb "calibrate"
3: if A$="N";jmp 3
4: ent "Continue calibration? (Y/N)",B$
5: if B$="Y";jmp -3
6: ent "Date",C$,"Time",D$
7: ent "Wafer number",E$
8: ent "Wafer type [P or N]",F$
9: ent "Wafer diameter [cm]",D
10: ent "Wafer thickness [mm]",r1
11: ent "Wafer mean resistivity [ohm cm]",r2
12: ent "Length of step [mm]",L
13: ent "Number of steps [even]",S
14: ent "Amplifier time constant [msec]",T
15: dsp "WAFER CENTERED?  LINEAR STAGE?";beep;stp
16: dim A[S+2],B[S+2],C[S+2],D[0:S+2],E[0:S+2],F[S+2],J[S+2],K[S+2],P[0:S+2]
17: 6→r0;0→I→M→Q→R→X→Y→Z;1→N;1000→J;(N-1-S/2)*L→P[N];100*L→A
18: dsp "BEAM MOVING TO 'START' POSITION"
19: 100*L*(S/2+1)→B;if B<4096;jmp 2
20: B-2047→B;7777→X
21: if B>2047;B-2047→B;7777→Y
22: dtoB→B;B+4000→Z;gsb "motor"
23: fmt 1,c5,c10;wrt 6.1,"Date:",C$
24: fmt 1,c5,c7,c27;wrt 6.1,"Time:",D$,"WAFER"
25: fmt 2,c25,c11,c13,c3;wrt 6.2,"Number  :",E$,"Type      :",F$
26: fmt 3,c25,f6.2,c3,c15,f7.3,c3
27: wrt 6.3,"Diameter:",D,"cm","Thickness:",r1,"mm"
28: fmt 4,c40,f8.3,c7;wrt 6.4,"Average resistivity:",r2,"ohm cm"
29: wrt 6
30: fmt 5,c41,f6.2,c3;wrt 6.5,"Length of step :",L,"mm"
31: fmt 6,c41,f6.0;wrt 6.6,"Number of steps:",S
32: wrt 6;wrt 6
33: fmt 7,c11,c9,c21,c10,c6,c14,c11
34: fmt 8,c14,c11,c15,c10,c9,c11,c10
35: wrt 6.7,"Location","I=0","dR(x)","Sum(Rdx)","rho","dR'(x)"," Sum(R'dx)"
36: wrt 6.8,"[mm fm center]","Volts","Ohms","Ohm-cm","Ohm-cm","Ohms","Ohm-cm"
37: wrt 6
38: if F$="N";9.182*3.6*r2*r2/(.05*D*r1)→r4
39: if F$="P";-9.182*1.36*r2*r2/(.05*D*r1)→r4
40: gsb "step"
41: fxd 1;dsp "BEAM IS",P[N],"mm FROM CENTER";gsb "meter"
42: if J[N]=99;fmt 1,4x,f6.2,4x,c8;wrt 6.1,P[N],"OVERLOAD";jmp 2
43: fmt 2,4x,f6.2,5x,f6.3;wrt 6.2,P[N],A[N]
44: P[N]+L→P[N+1];if (N+1→N)<S+2;jmp -4
45: wtb 6,27,10;J[S/2+1]→r5;P[N]-L→P[N];N-1→N;ent "Current [mA]",Q
46: ent "Calibrate? (Y/N)",A$
47: if A$="Y";gsb "calibrate"
48: if A$="N";jmp 5
49: ent "Continue calibration? (Y/N)",B$
50: if B$="Y";jmp -3
51: jmp 2
```

EXPLANATION OF PROGRAM

LINE	PURPOSE
0	Reserves memory space for temporary data (date, responses to questions, etc.).
1-5	If the response is YES, triggers the meter at one-half second intervals for 15 seconds to permit selection of optimum meter range.
6-14	Enters data needed to identify the wafer and its characteristics.
15	Reminds the operator to center the wafer and energize the linear stage before beginning measurements.
16,17	Reserves memory space for data and assigns initial values to variables.
18-22	Moves stage to starting position.
23-32	Prints wafer identification and characteristics.
33-37	Prints headings for data.
38,39	Calculates constant for N or P-type material.
40-44	Steps the stage through the number of positions prescribed in steps 12 and 13, reads the meter at each position, and prints the position of the stage and the photovoltage in two columns.
45	Assigns values to variables; enters magnitude of current applied to wafer.
46-51	If response is YES, triggers the meter at one-half second intervals for 15 seconds to permit selection of optimum meter range.

```
52: gsb "backstep"
53: fxd 1;dsp "BEAM IS",P[N],"mm FROM CENTER";gsb "meter"
54: if J[N]=99;fmt 1,22x,c8;wrt 6.1,"OVERLOAD";jmp 2
55: fmt 2,23x,f6.3;wrt 6.2,B[N]
56: wtb 6,27,10,27,10;P[N]-L→P[N-1];if (N-1→N)>=1;jmp -4
57: J[S/2+1]→r6;fmt 3,16x,"x10",f2.0,3x,"x10",f2.0;wrt 6.3,r5,r6
58: wtb 6,27,10,27,10,27,10;fmt 4,22x,"I=",f5.3,"mA";wrt 6.4,Q
59: wtb 6,27,77,10,10;1→N;0→r7
60: -1*abs((B[S/2+1]*10^r6-A[S/2+1]*10^r5)/(.001*Q))→C[S/2+1]
61: -1*abs((B[N]*10^r6-A[N]*10^r5)/(.001*Q))→C[N]
62: 1/(1-(P[N]/(5*D))^2)→J[N];C[N]/J[N]^2→K[N]
63: L/10*r4*J[N]*A[N]*10^r5/C[N]→D[N];D[N]+D[N-1]→D[N]
64: if P[N]>=-16;if P[N]<=16;D[N]+r7→r7;R+1→R
65: L/10*r4*1/J[N]*A[N]*10^r5/C[S/2+1]→E[N];E[N]+E[N-1]→E[N]
66: if (N+1→N)<S+2;gto 61
67: r2-r7/R→r7;1→N;fmt 1,32x,3f9.3,3x,f9.4,f9.3
68: wrt 6.1,C[N],D[N],D[N]+r7→F[N],K[N],E[N]
69: if F[N]>M;F[N]→M
70: if F[N]<J;F[N]→J
71: if (N+1→N)<S+2;gto 68
72: dsp "BEAM RETURNING TO WAFER CENTER"
73: 100*L*S/2→C;0→X→Y→Z;if C<4095;jmp 2
74: C-2047→C;3777→X
75: if C>2047;C-2047→C;3777→Y
76: dtoC→Z;gsb "motor"
77: dsp "To plot, change paper in printer.";beep;stp
78: fxd 1;dsp "Rmin=",J,"Rmax=",M,"Ymin=?";ent "",J
79: fxd 1;dsp "Rmin=",J,"Rmax=",M,"Ymax=?";ent "",M
80: cll 'form'(9.5,13,13)
81: cll 'psiz'(9.75,8,3,.5)
82: cll 'scl'(-26,25,J-(M-J)/5,M+(M-J)/10)
83: cll 'xaxis'(J-(M-J)/10,5,-25,25)
84: cll 'yaxis'(0,(M-J)/10,J,M)
85: -25→I;fmt f3.0,z
86: cll 'move'(I,J-(M-J)/10);cll 'space'(-1);cll 'skip'(1)
87: wrt 6,I;if (I+5→I)<-5;jmp -1
88: cll 'move'(I,J-(M-J)/10);cll 'space'(-1);cll 'skip'(1)
89: fmt f2.0,z;wrt 6,I;if (I+5→I)<=25;jmp -1
90: cll 'space'(-32);cll 'skip'(1);wrt 6,"DISTANCE FROM CENTER OF WAFER-mm"
91: J→I;fmt 1,f6.1,z
92: cll 'move'(0,I);wrt 6.1,I;jmp (I+(M-J)/5→I)>M
93: cll 'move'(-1.5,M);cll 'skip'(-1);wrt 6,"OHM-CM"
94: cll 'move'(P[1],F[1]);1→N;cll 'char'(46,5,3)
95: cll 'fplt'(P[N],F[N],111);jmp (N+1→N)>S+1
96: cll 'move'(-8,J);cll 'skip'(8);wrt 6,"RESISTIVITY VERSUS POSITION"
97: fmt c44,c12,14x,c8,c8;wrt 6,"WAFER: ",E$,C$,D$
98: wtb 6,13;dsp "END";beep;gto 77
```

LINE	PURPOSE
52-56	Reverses direction of stage and steps it through the same positions covered in steps 40-44, reads the meter at each position, and prints the photoconductivity in a third column, starting at the bottom of the column and moving up.
57-58	Prints the current magnitude and the multipliers for the photovoltage and photoconductivity columns.
59	Moves to first row of data and sets counters.
60-71	Calculates change in photoresistance and resistivity for both the actual and idealized cases and prints these values in the next five columns.
72-76	Returns laser beam to center of wafer.
77-79	If plot of resistivity is desired, displays minimum and maximum values of resistivity and requests operator to set abscissa limits.
80-84	Locates plot on page and draws x and y axes.
85-90	Scales and labels x axis.
91-93	Scales and labels y axis.
94,95	Plots resistivity, F[N], versus position, P[N].
96,97	Prints title of graph.
98	End statement.

```
99: "calibrate":
100: 0→I
101: wrt 723,"O260TAT240T";wait 500;jmp (I+500→I)=15000
102: 0→I;ret
103: "meter":
104: fmt ;wait 5*T
105: wrt 723,"O260TAT240TAT";red 723,E
106: wrt 723,"O240TCT";red 723,F
107: E-10000→E;otdE→E;E-6int(E/16)-60int(E/256)→E
108: if F>10000;F-10000→F
109: if F>1000;F-1000→F;99→J[N];jmp 8
110: if F>100;F-100→F;1→G;jmp 2
111: -1→G
112: if F>10;F-10→F;1→K;jmp 2
113: 0→K
114: F-7→J[N]
115: if Q=0;G*(K+E/1000)→A[N];jmp 2
116: G*(K+E/1000)→B[N]
117: ret
118: "motor":
119: fmt 3,c,f4.0,c,z;wrt 723.3,"O160TK",X,"TO40T"
120: wrt 723.3,"O160TK",Y,"TO40T"
121: wrt 723.3,"O160TK",Z,"TO40T"
122: ret
123: "step":
124: 0→X→Y;if A<2048;jmp 2
125: A-2047→A;3777→Y
126: dtoA→Z;gsb "motor"
127: ret
128: "backstep":
129: 0→X→Y→Z;if A<2048;jmp 2
130: A-2047→A;7777→Y
131: dtoA→Z;Z+4000→Z;gsb "motor"
132: ret
133: "form":
134: wtb r0,27,77
135: wtb r0,27,84
136: wtb r0,27,87,int(120*p1/64),120*p1
137: wtb r0,27,76,int(96*p2/64),96*p2
138: wtb r0,27,70,int(96*p3/64),96*p3
139: ret
140: "psiz":
141: p1→H;p2→W
142: wtb r0,27,79,int(p4*120/64),p4*120,int(p3*96/64),p3*96
143: ret
144: "scl":
145: 120W/(p2-p1)→U
146: 96H/(p4-p3)→V
147: p1→X;p3→Y
148: ret
```

LINE	PURPOSE
99-102	"Calibrate" subroutine triggers meter at one-half second intervals.
103-117	Subroutine for reading meter.
118-122	Moves stage X+Y+Z steps using values of X, Y, and Z determined by main program or "step" subroutine.
123-127	Moves stage forward A steps; value of A determined by main program.
128-132	Moves stage A steps in reverse.
133-139	Enters dimensions of page.
140-143	Locates graph on page.
144-148	Scales graph.

```
149: "xaxis":
150: wtb 6,27,46,95,0,5,9
151: wtb 6,27,65,int((p3-X)U/64),int((p3-X)U),int((p1-Y)V/64),int((p1-Y)V)
152: p3→p5;wtb 6,43;wtb 6,8
153: wtb 6,27,114,int(p2U/64),int(p2U),0,0;wtb 6,43,8;jmp (p5+p2→p5)>=p4
154: ret
155: "yaxis":
156: wtb 6,27,46,124,0,3,0
157: wtb 6,27,65,int((p1-X)U/64),int((p1-X)U),int((p3-Y)V/64),int((p3-Y)V)
158: p3→p5;wtb 6,43;wtb 6,8
159: wtb 6,27,114,0,0,int(p2V/64),int(p2V);wtb 6,43,8;jmp (p5+p2→p5)>=p4
160: ret
161: "move":
162: wtb 6,27,65,int((p1-X)U/64),int((p1-X)U),int((p2-Y)V/64),int((p2-Y)V)
163: ret
164: "space":
165: if p1<0;gto +2
166: wtb r0,32;jmp 2((p1-1→p1)=0)
167: wtb r0,8;jmp (p1+1→p1)=0
168: ret
169: "skip":
170: if p1<0;gto +2
171: wtb r0,10;jmp 2((p1-1→p1)=0)
172: wtb r0,27,10;jmp (p1+1→p1)=0
173: ret
174: "fplt":
175: wtb 6,27,97,int((p1-X)U/64),int((p1-X)U),int((p2-Y)V/64),int((p2-Y)V)
176: if p3=46;wtb 6,27,82,0,0,0,6
177: wtb 6,p3;wtb 6,8
178: if p3=46;wtb 6,27.82,0,0,63,-6
179: ret
180: "char":
181: if p2=0;5→p2;0→p3
182: wtb 6,27,46,p1,int(p2/64),p2,p3
183: ret
```

LINE	PURPOSE
149-154	Draws x axis.
155-160	Draws y axis.
161-163	Moves plotter pen to specified position, p1, p2, on graph.
164-168	Moves plotter horizontally.
169-173	Moves plotter vertically.
174-179	Plots data points and draws lines between them.
180-183	Specifies character to be used in drawing lines between data points.

APPENDIX B

Defects in PN Junctions and MOS Capacitors Observed Using Thermally Stimulated Current and Capacitance Measurements

by

Martin G. Buehler

Two measurement methods are described which detect and characterize defects which can control such device characteristics as lifetime and junction leakage. The methods can be used as diagnostic tools in the fabrication of bipolar and MOS devices. The number of different kinds of defects and their densities may be obtained with little effort and simple apparatus. Positive identification of these defects may be obtained with more effort and more sophisticated apparatus. Of more importance, the measurements characterize defects in an environment which is identical to that of the finished product. Thus, the answers derived are directly applicable to process control and device design.

These methods involve thermally stimulated capacitance and current measurements which utilize the ability of defects in the vicinity of a p-n junction or in an MOS capacitor to trap holes or electrons and emit them after receiving sufficient thermal energy. Values for defect densities, energy levels, and emission rates can be derived from these measurements. The limit of detectability can be as low as 10^{10} defects/cm^3. These values provide sufficient information to positively identify the defects.

Three vehicles are used to illustrate the methods: a gold doped n^+-p diode, a p^+-n diode with a process-induced defect center, and a gold doped n-type MOS capacitor. Two cryostats are described which have a maximum heating rate of 10 K/s.

The class of measurements that will be presented are known as thermally stimulated current and capacitance measurements. These measurements detect defects in the space charge region of p-n junctions and MOS capacitors. The defects may be intentionally introduced, such as gold, or they may be processed induced defects or radiation induced defects. The introduction of these defects has the effect of either changing the resistivity of silicon or of lowering its lifetime and thereby increasing the leakage currents in junctions. The thermally stimulated current and capacitance measurements are very sensitive to the presence of defect centers, for they are able to detect as little as one defect center in a trillion silicon atoms.

The measurements presented here are for defect centers observed in silicon; however, defects have been observed by these measurements in other semiconductors. Compared to other methods, these measurements are the most sensitive and the analysis is rapid.

In this presentation the physics of the measurement is discussed first, followed by

various practical examples, and finally the measurement apparatus is described.

The key features of the thermally stimulated current and capacitance measurements are shown in this energy band diagram. [Figure 1] In this *p*-type semiconductor, acceptors have an electron and are negatively charged. For conceptional purposes these donor defects may be thought of as the gold donor defect in *p*-type silicon. These defects have an energy level, E_t, close to the valence band. Defects communicate with the valence band and conduction band through either electron capture, electron emission, hole capture, or hole emission [indicated by arrows, in Figure 1, from left to right]. Donor defects are either positive, when a hole resides at the center, or neutral, when an electron resides at the center.

In the space-charge region the emission rates govern the charge state of the defect center. From energy considerations the hole emission rate is much faster than the electron emission rate. Thus, the defect has no charge in the space-charge region under steady state conditions. In the neutral region the charge state is governed by the Fermi energy level, E_f, which dictates that the defect be positively charged.

In order to detect defect centers, there must be a change in charge states between centers in the space-charge region and those in the neutral region. This point will be amplified later.

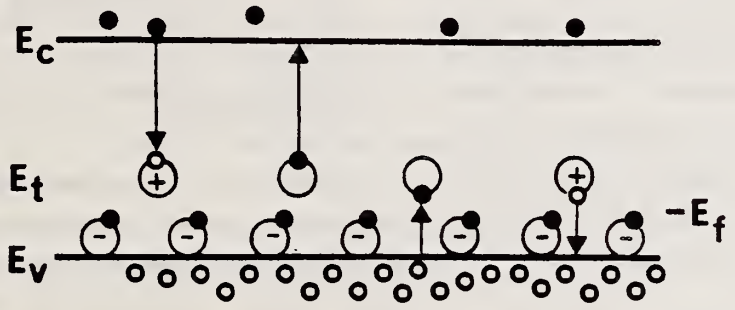


Figure 1. Emission and capture processes at a defect center in the energy gap of a semiconductor.

The emission rate for the holes and electrons depends on the defect energy level. The mathematical relationship is shown next. [Figure 2] This expression pertains to holes or electrons depending on whether the subscript *x* is *p* or *n*. The expression indicates that the emission rate depends on a pre-exponential B-coefficient, times the temperature T squared, times the negative exponential of the energy needed by a hole or electron to escape to its respective band edge normalized

EMISSION RATE

$$e_x = B_x T^2 \exp(-\Delta E_x / kT)$$

HOLE EMISSION (x = p)

ELECTRON EMISSION (x = n)

Figure 2. Emission rate expressions

by kT, where k is the Boltzmann constant.

The nature of the measurement is illustrated next [Figure 3] by this schematic representation of an n^+-p junction with two donor defects on the lightly doped p-type side of the junction [defect indicated by a star]. With zero bias applied to the junction, the space-charge region is very small, extending from the junction to the dashed line [Figure 3A]. The n^+ region is assumed to be so heavily doped that the space-charge penetration into this region may be neglected. In the neutral region, the negative charge on the acceptor atoms is neutralized by valence-band holes, and the positive charge on the donor defects is neutralized by conduction-band electrons.

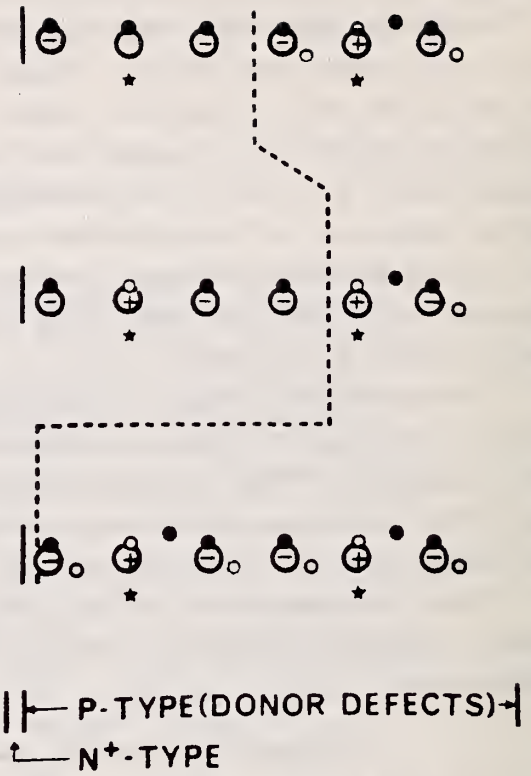
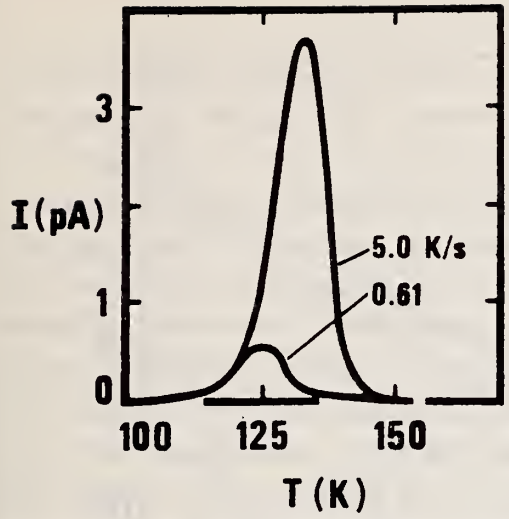


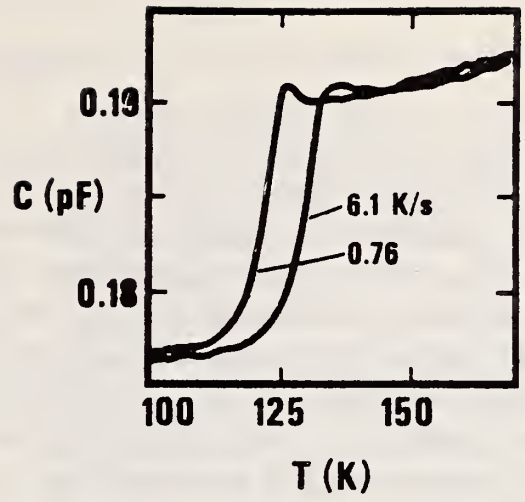
Figure 3. Charge state of defect centers in n^+-p junction.

Under zero bias the junction is now lowered to liquid nitrogen temperature. Now, at this temperature, a reverse bias is applied to the junction which widens the space-charge region as illustrated here [Figure 3B]. Valence-band holes and conduction-band electrons are removed from the space-charge region. At this temperature the hole remains on both defect centers: the one in the space-charge region and the one in the neutral region.

As the temperature of the junction is increased, a critical temperature is reached, called the emission temperature, at which the hole on the defect in the space-charge region receives sufficient thermal energy to be released to the valence band. Through this process the defect center has changed charge state from positive to neutral and the release of the hole constitutes a current which can be measured in an external circuit. The change in charge state means that the space-charge region must shrink so as to maintain charge balance [indicated in Figure 3C]. This motion of the space-charge region constitutes a change in the junction capacitance which can also be measured in an external circuit. This example illustrates the case of the gold donor in a silicon n^+-p junction.

Experimental results for such a junction will be shown next [with use of Figure 4]. The junction was first cooled to liquid nitrogen temperature. The donors were charged with holes by zero biasing the junction. After a reverse bias of 22.5 volts was applied, the junction was heated slowly at 0.61 kelvin per second and the current measured [Figure 4A]. The junction was again cooled to liquid nitrogen temperature and defects charged, but this time the junction was heated at 5 kelvin per second.





A B

Figure 4. Response of a gold doped n^+-p junction.

These dynathermal or dynamic-temperature measurements indicate that hole emission from the gold donor is heating-rate dependent, for at the slower heating rate the peak occurs at 125 kelvin and at the higher heating rate it occurs at 134 kelvin. Because the current response is governed by the rate at which holes are emitted per unit time, the sensitivity of this measurement depends on the heating rate. For a high heating rate of 10 kelvin per second it is possible with our equipment to detect 10^{10} defects/cm^3 or one defect center in a trillion silicon atoms.

Next [Figure 4B] is shown the dynathermal capacitance response of the gold donor. This step in the capacitance response is directly related to the number of gold atoms which in this case is about 10^{15}/cm^3. Because the capacitance response is governed by the number of the holes emitted, the magnitude of the capacitance step is not heating rate dependent. For our equipment, defect centers are detectable if their density is greater than one defect in five hundred background dopant atoms.

For the non mid-gap defect shown here, the capacitance measurement is by far the easier in terms of the experimental apparatus and theoretical interpretation. For example, simple cryostats may be used, for icing is not a problem and low heating rates may be used. However, as will be shown, the dynathermal current measurements are superior when evaluating mid-gap defect centers which are the source of junction leakage.

The next example is a process-induced defect center in a silicon p^+-n junction. This defect was unintentionally introduced into the junction. It resulted from the fabrication process. The dynathermal current and capacitance response for this defect [Figure 5] indicates that this center has two energy levels, as indicated by the emission processes at 150 and 225 kelvin. This example allows a comparison between the dynathermal response of a non-mid-gap energy level and a mid-gap energy level. The non-mid-gap energy level is initially completely full of electrons and finally completely emptied of electrons. The mid-gap energy level is initially completely full of electrons but after the electrons have begun to be emitted, this level begins to generate both electrons

and holes. It is the leakage source for the junction as indicated by the rapid rise in the current with temperature. This shoulder response of the dynathermal current is a key to its rapid identification. As will be shown this response is quite different from the gold acceptor response.

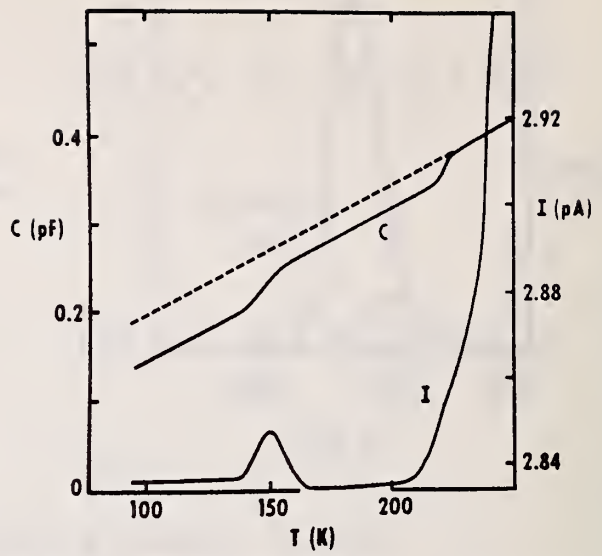


Figure 5. Response of a p^+-n junction with process-induced defect centers.

Before this center is discussed further, a limitation of the measurements is discussed [with the use of Figure 6]. The ability of these measurements to detect defects depends on whether the defects change charge state. This in turn depends on the position of the defect energy level in the energy gap. As an example, consider an n-type semiconductor [Figure 6A] with an acceptor defect center whose energy level is located well below mid-gap. In the neutral region, denoted by electrons in the conduction band, the center is negatively charged. In the space-charge region, denoted by the absence of electrons in the conduction band, the electron sticks on the center for at reasonable temperatures the electron cannot receive enough thermal energy to be excited to the conduction band. This defect center does not change charge state and is therefore not detectable by these measurements.

For an energy level at mid-gap, the center is initially charged with an electron but in its final state it acts as a generation site emitting holes and electrons [Figure 6B]. Its final charge state is governed by these emission rates which dictate its detectability.

For an energy level above mid-gap, centers are initially fully charged with electrons and finally fully discharged [Figure 6C]. These centers have optimum detection conditions.

In summary [Figure 6D], the ability to detect defects in n-type silicon depends on the position of the energy level of the defect center. If the energy level lies in the lower half of the gap, then no measurement is possible (M=0). If the level is in the upper half of the energy gap then the measurement has the best chance of succeeding (M=1).

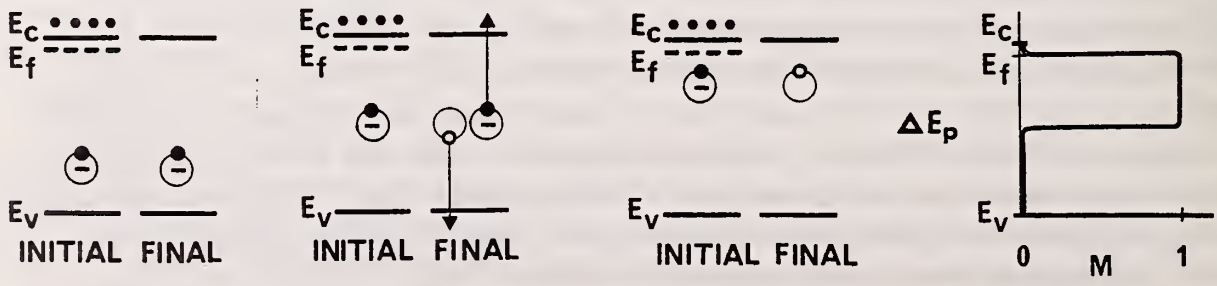


Figure 6. Measurement detectability of acceptor defect centers located at different energy levels.

If the level lies above the Fermi level, E_f, detectability is poor because the center is initially not charged with electrons.

The three kinds of measurement methods used to characterize defects are discussed now with respect to the process-induced defect in a silicon p^+-n junction [Figure 5]. The measurements shown here are dynathermal measurements. The emission temperature and the heating rate are initial clues to the atomic identity of the defect center. The emission temperature is defined by the current peak or the maximum capacitance slope. A more definitive analysis of the emission rate, which involves the energy level determination, follows from isothermal capacitance measurements. In this measurement, made at a fixed temperature, the capacitance time constant is determined as the capacitance goes from its initial state to its final state. Measurements are taken at various temperatures and from the analysis comes both the energy level and the pre-exponential B-coefficient. Such measurements were used to evaluate the electron emission rate for the 150 kelvin emission process.

The emission process at 225 kelvin is a mixture of both electron and hole emission. To evaluate these emission rates both isothermal capacitance and steady state leakage measurements are needed. The results of such evaluations are shown next [Figure 7] for the two emission processes. The non-mid-gap electron emission observed at 150 K is characterized by this emission rate, [$e_n = 4.1 \times 10^3\ T^2 \exp(-0.23/kT)$], and its energy level is in the middle of the upper half of the energy gap. The emission process observed at 225 K is given by these electron and hole emission rates, [$e_n = 3.5 \times 10^8\ T^2 \exp(-0.61/kT)$ and $e_p = 3.4 \times 10^6\ T^2 \exp(-0.55/kT)$], and their energy level is near mid-gap. The defect density, N_t, for the two levels is the same within experimental error since both emission processes are coupled to the same defect center.

$T_e = 150$ K for $\beta_e = 7.5$ K/s

$e_n = 4.1 \times 10^3\ T^2 \exp(-0.23/kT)$

$N_t = 3.0 \times 10^{12}\ cm^{-3}$

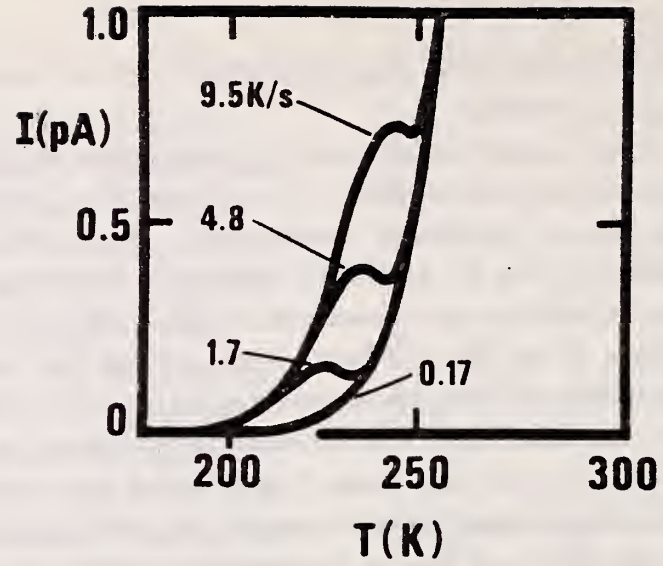
$T_e = 225$ K for $\beta_e = 4.2$ K/s

$e_n = 3.5 \times 10^8\ T^2 \exp(-0.61/kT)$

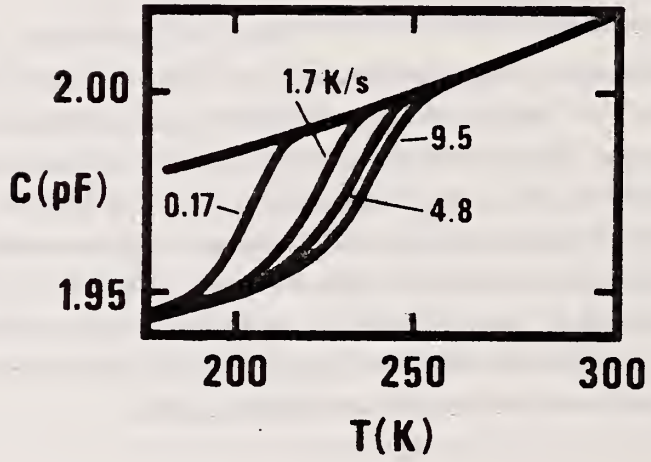
$e_p = 3.4 \times 10^6\ T^2 \exp(-0.55/kT)$

$N_t = 2.9 \times 10^{12}\ cm^{-3}$

Figure 7. Emission rate expressions and defect density for the process-induced center shown in Figure 5.



A



B

Figure 8. Response of a gold doped p^+-n junction.

The shoulder shape of the dynathermal current response is a unique signature for the process-induced defect center [Figure 5]. This shape is distinctly different from the dynathermal current response for the gold acceptor defect in a silicon p^+-n junction shown next [Figure 8A]. This response shows a peak and valley before it goes into steady state leakage. This dramatically demonstrates how dynathermal current measurements can be used to identify mid-gap defect centers. The currents shown here were measured at various heating rates. If the heating rate is slow enough, [0.17 K/s], electron emission is difficult to detect and the current response is essentially the steady state leakage response. The capacitance response is shown next [Figure 8B] for various heating rates. From this shift in characteristics the gold density was found to be about 3 percent of the background donor density.

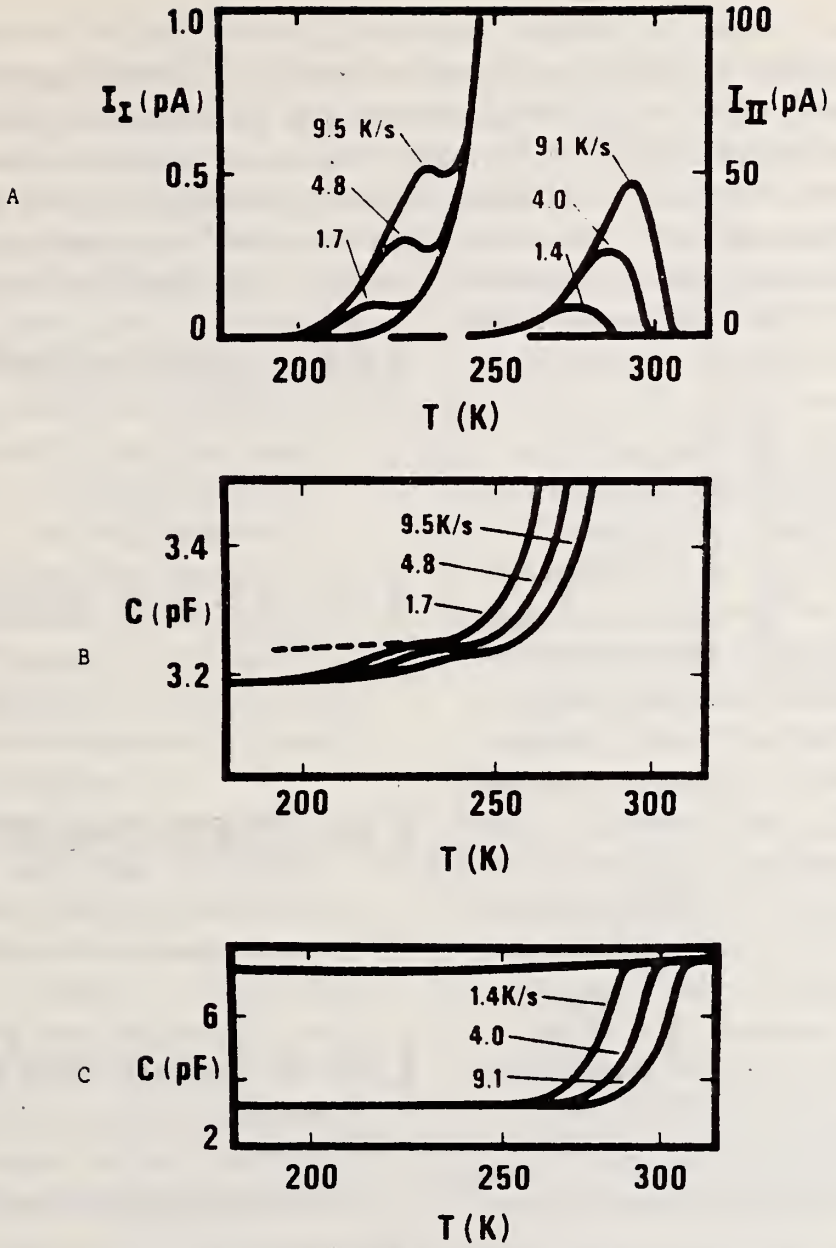


Figure 9. Response of a gold doped *n*-type MOS capacitor.

The current and capacitance response for a gold doped silicon p^+-n junction is identical to the initial response of a gold doped *n*-type MOS capacitor. The dynathermal current response of such an MOS capacitor is shown next [Figure 9A] for various heating rates. The phase I response has a peak and valley characteristic indicative of the gold acceptor. This response, which is dominated by electron emission, is scaled according to the left hand axis. In addition to phase I there is a second phase. The phase II response, which is dominated by hole emission, is scaled according to the right hand axis. Notice that once equilibrium has been reached [at high temperatures], no current flows through the MOS capacitor.

The phase I capacitance response is shown next [Figure 9B] and from this step in the

response the gold density was found to be about 4 percent of the background donor density. Once the gold center begins to act as a generation site, the capacitance begins to change rapidly. By rescaling the capacitance response, the overall response is shown next [Figure 9C] where phase I response is no longer visible. The phase II response is clearly evident. Once the capacitance reaches equilibrium inversion, no further change is noted. This point corresponds to cessation of current flow through the capacitor.

The physics of this measurement is explained in the following schematic diagram of an MOS capacitor [Figure 10]. A bias has been applied to the metal gate so as to invert the oxide-silicon interface represented by the hole [at the oxide-silicon interface, Figure 10A]. A space-charge region exists free of conduction-band electrons and valence-band holes [from the interface to the dashed line]. This region is followed by a neutral region. Acceptor defects are located at three positions [indicated by stars]. This condition is established at room temperature and then the MOS capacitor is cooled to liquid nitrogen temperature. At this low temperature the applied bias is changed so that the space-charge region is increased [Figure 10B]. This gold center [middle one] has been effectively charged with an electron which sticks since at this low temperature it does not receive enough thermal energy to be released.

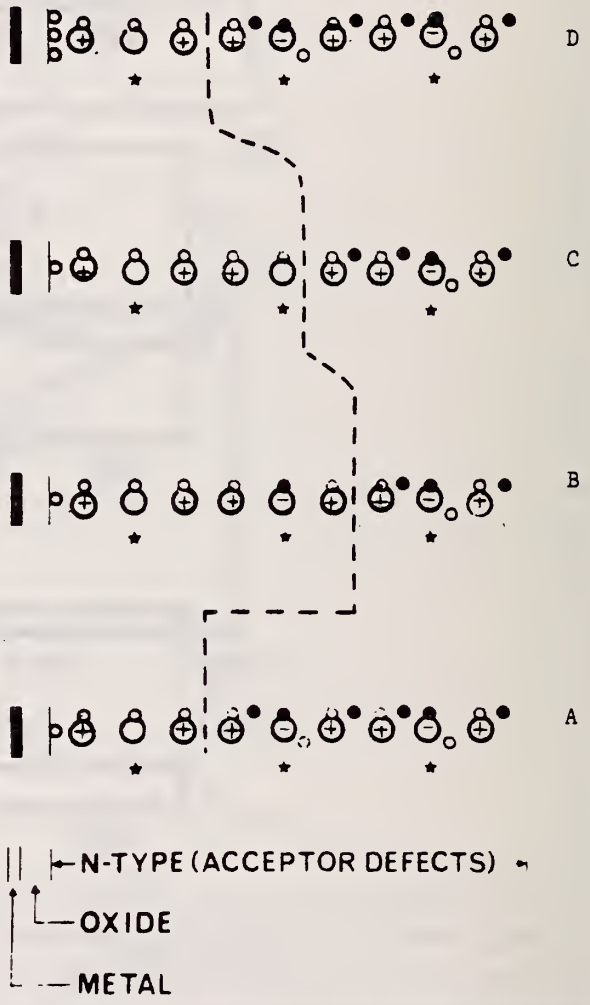


Figure 10. The charge state of defect centers in an *n*-type MOS capacitor.

As the temperature is increased, the electron is emitted and the space-charge region shrinks ever so slightly in order to maintain charge balance [Figure 10C]. This is the phase I response, which is dominated by electron emission.

As the temperature continues to rise, these gold defects act as generation sites emitting electrons and holes. Emitted electrons are swept by the electric field to the neutral region; whereas, emitted holes are swept to the oxide-silicon interface where they increase the hole density. This is the phase II response which is dominated by hole emission. As holes appear at the oxide-silicon interface, the space-charge region shrinks so as to maintain charge balance. The space-charge region continues to shrink until equilibrium inversion conditions are established [Figure 10D].

A brief review of the MOS capacitor dynathermal response is presented next [Figure 11]. This current response [Figure 11A] illustrates the turn-on of phase I, the phase I emission temperature [T_{eI}], the phase II emission temperature [T_{eII}], and final equilibrium [zero current]. These four critical temperatures [indicated by the dashed lines] are related to the capacitance response as shown here [Figure 11B]. The phase I turn-on, the transition between phases, and final equilibrium are related to the MOS capacitance gate voltage characteristics [Figure 11C]. The room temperature, high frequency characteristics are shown by the heavy line. Recalling the measurement sequence, gate bias V_{g1} is first applied at room temperature and then the capacitor is lowered to liquid nitrogen temperature. Gate bias V_{g2} then biases the MOS capacitor into deep depletion. With V_{g2} applied, the temperature is increased and during phase I, electrons are emitted. As the temperature continues to rise, holes are pumped into the oxide-silicon interface until the equilibrium inversion condition is achieved.

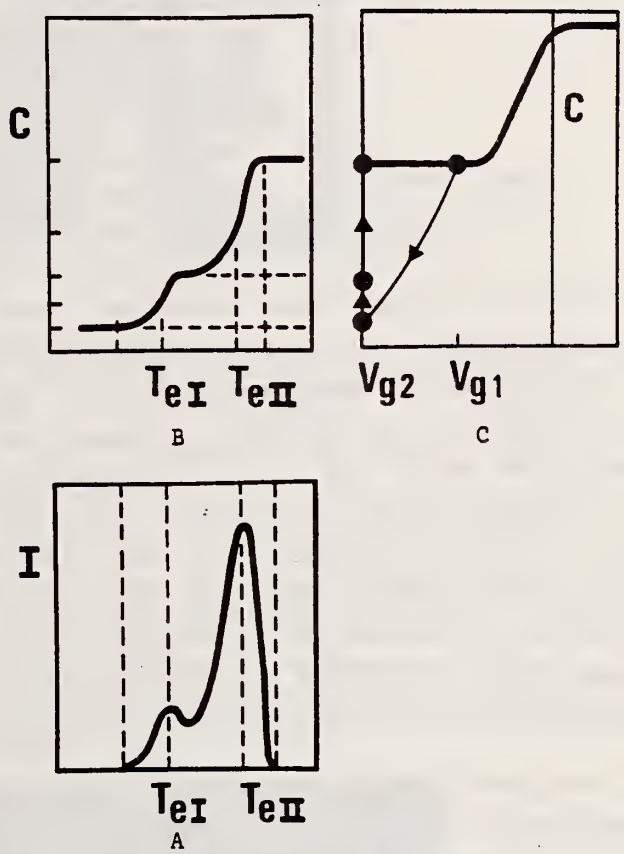


Figure 11. A schematic representation of the MOS capacitor response shown in Figure 9.

The dynathermal measurements show great promise in being able to identify the atomic nature of defects found in the space-charge region of *p-n* junctions and MOS capacitors. A catalog of defects might take the following form [Figure 12]. Here the defect energy level relative to the appropriate band edge has been plotted with respect to its phase I emission temperature for a heating rate of 1 kelvin per second. The dashed lines are related to the emission rate B-coefficient and the heating rate. For example, the gold donor [hole emission] has an emission temperature of 128 kelvin for a heating rate of 1 K/s; whereas, for a heating rate of 10 K/s it has a 136 kelvin emission temperature. In addition to the process-induced defect centers and the gold centers, radiation-induced defect centers are also shown. These centers were generated by electron irradiation or by neutron irradiation. Some centers have the same energy level but different B-coefficients and thus have different emission temperatures. Other centers have the same emission temperatures but different energy levels. If they are non-mid-gap centers, they can be identified by determining their energy levels from isothermal capacitance measurements. If they are mid-gap centers, then the shape of the dynathermal current response can be used to establish their identity. For example

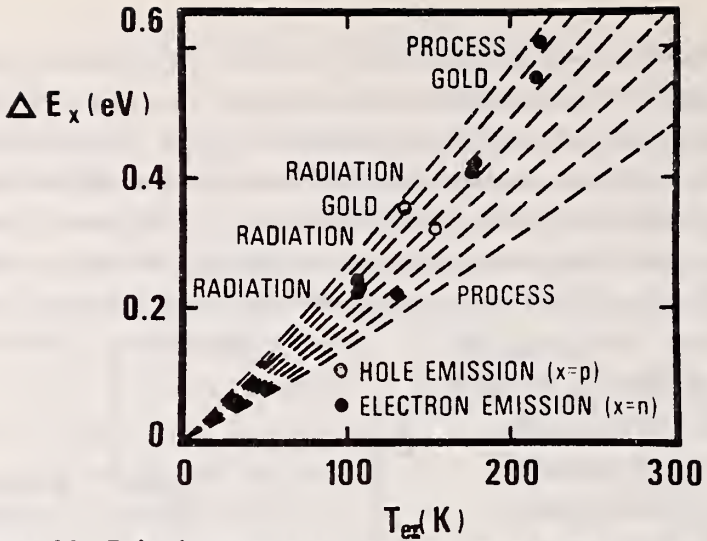


Figure 12. Emission temperatures of various defect centers in silicon for a heating rate of 1 K/s.

recall that the process-induced defect had a shoulder response [Figure 5] whereas the gold acceptor defect had a peak and valley response [Figure 8A].

The experimental apparatus used in these experiments is capable of measuring currents one hundred times less than a picoampere and of measuring capacitance changes one hundred times smaller than a picofarad at heating rates as high as 10 kelvin per second. This is achieved in part by mounting *p-n* junctions or MOS capacitors on a TO-5 header. The unit under test is mounted on a ceramic slab as shown here [Figure 13]. The ceramic slab is gold coated on both sides which allows easy alloying. On its top side the gold coating is broken so that a temperature sensing diode mounted here is electrically isolated from the unit under test. The temperature sensing diode is forward biased at 10 microamperes, and its forward voltage is proportional to the temperature.

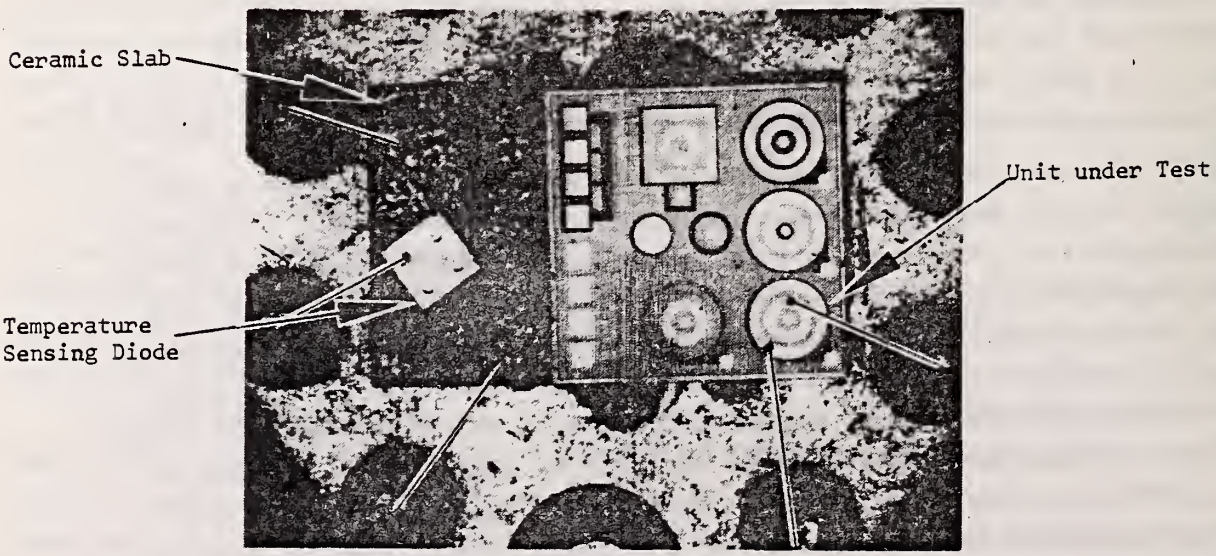


Figure 13. Sample mounting scheme in a 10-pin TO-5 header.

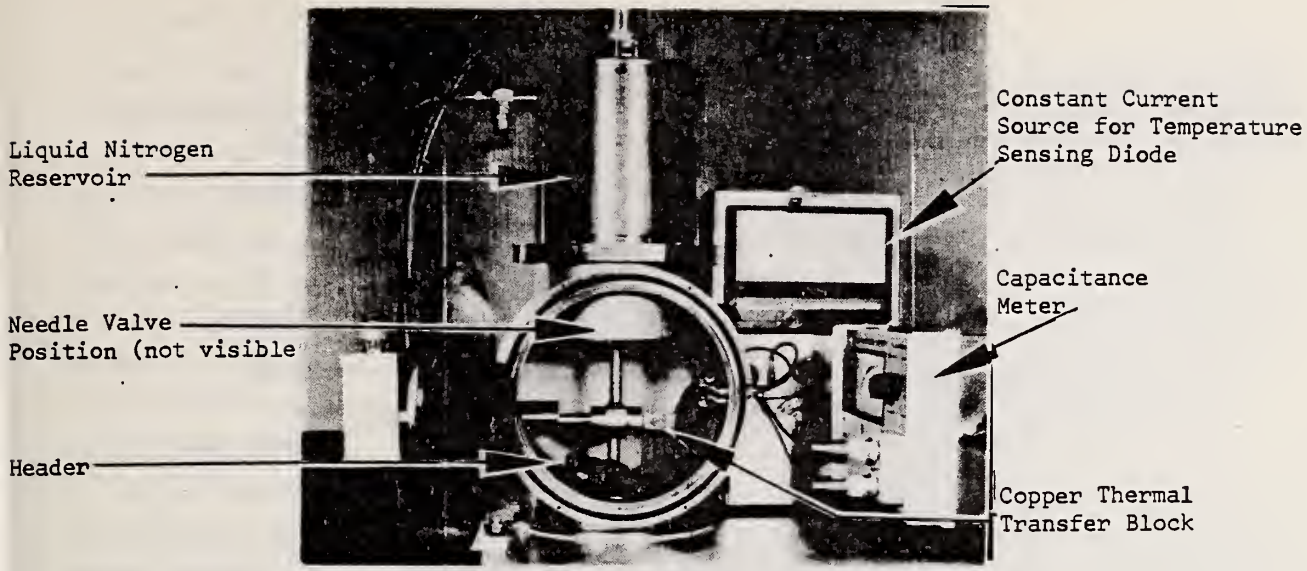


Figure 14. Cryostat number 1.

Two experimental systems are in current use in our laboratory. The first system [Figure 14] is capable of both dynathermal and isothermal measurements. It consists of a liquid nitrogen reservoir with a needle valve at the bottom of the reservoir which allows the liquid nitrogen to flow around a copper thermal transfer block and out of the cryostat. Within the copper block is a 150 watt heater. Under test conditions the TO-5 header is mounted in the hole in the copper block. The chamber is evacuated using a roughing pump. This procedure prevents icing problems. Dynathermal measurements consist of cooling the unit under test to liquid nitrogen temperature, charging the defects using a proper bias sequence, shutting off the liquid nitrogen, heating the copper block, and recording the current or capacitance response.

The second and simpler system that has only dynathermal capabilities is shown here [Figure 15]. It consists of a funnel which directs liquid nitrogen into the bellows area where the TO-5 header is mounted. The cap is raised into position and the chamber is evacuated. The capacitance meter is located close to the apparatus to minimize lead length. A closer view [Figure 16] reveals the TO-5 header positioned into the base of a copper thermal transfer block. The header looks directly into the end of a 150 watt heater which is silver soldered into the copper block. The heater leads are taken out of the funnel and thereby shielded from the TO-5 header. This cryostat features quick loading and unloading capabilities. A dynathermal measurement can be performed in well under 10 minutes.

In conclusion, this class of measurements reveals defects in the space-charge region of p-n junctions and MOS capacitors if the defects can be charged and discharged. This means that defects must lie in the mid to upper half of the energy gap in n-type silicon, and must lie in the mid to lower half of the gap in p-type silicon. However, this is not a handicap in that these measurements can detect mid-gap leakage centers

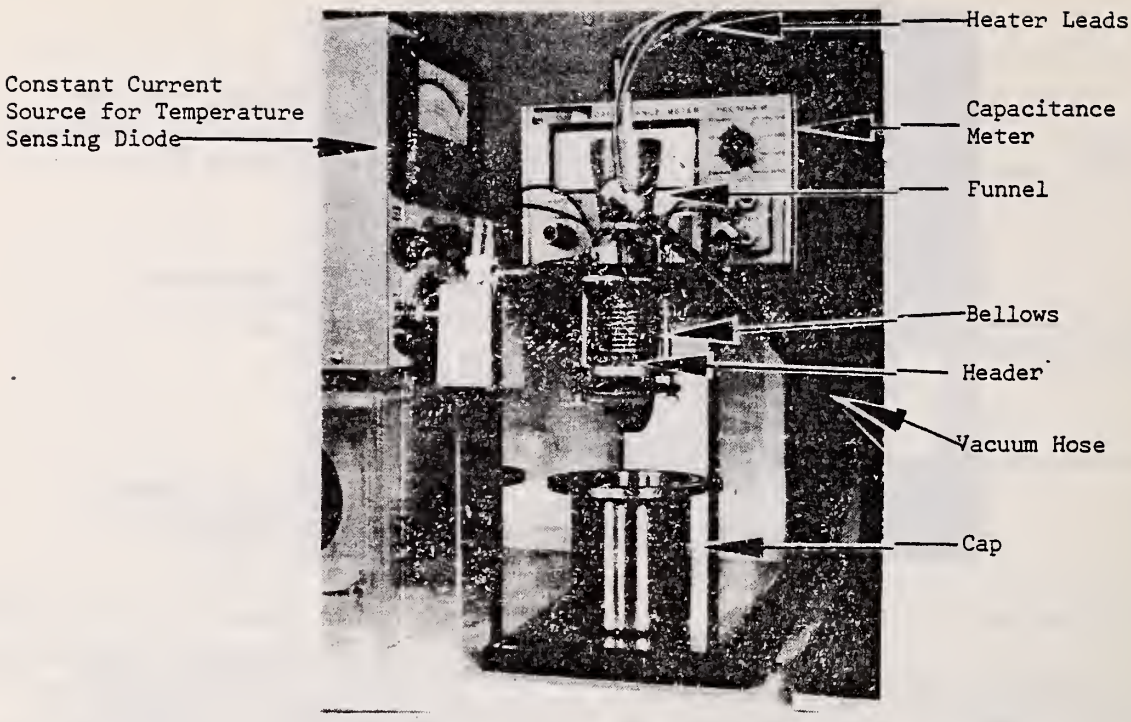


Figure 15. Cryostat number 2.

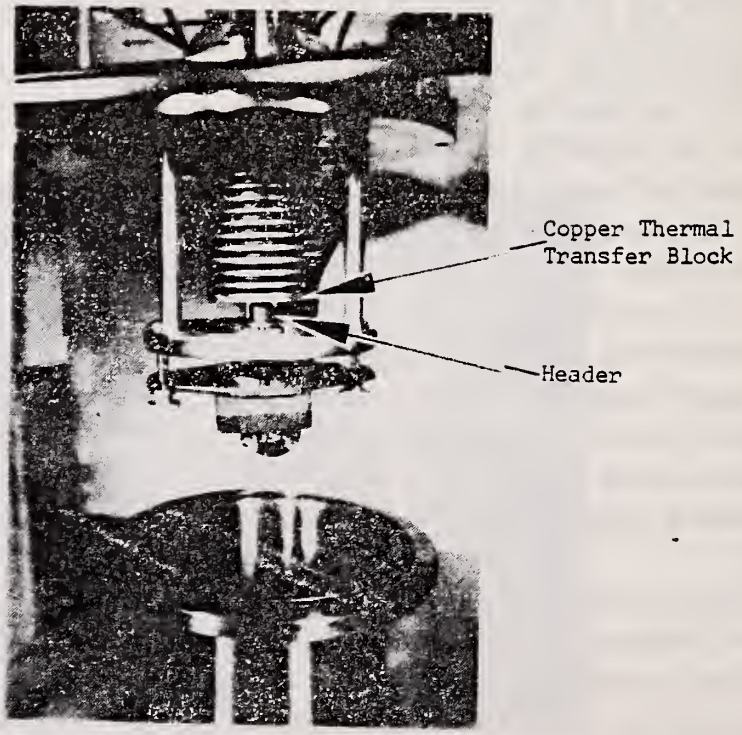


Figure 16. Close up view of cryostat number 2.

in both *n*- and *p*-type silicon. The detectability of the defects is one defect in a trillion silicon atoms when measuring current, and when measuring capacitance it is one defect in five hundred dopant atoms. These estimates are conservative for ultimate detectable limits may be lower. Dynathermal measurements are useful in providing a quick thermal scan which reveal the variety of emission processes present and the density of each. From a defect catalog the atomic nature can be tentatively identified. Mid-gap leakage centers that have a unique dynathermal current signature can be readily identified. For non mid-gap centers, isothermal capacitance measurements can be used to determine its energy level. Using a defect catalog leads to positive identification.

In our laboratory, work is currently under way to catalog more defect centers by intentionally doping silicon with various defect centers. In addition, work is directed toward enhancing the usefulness of these measurements. For example, the measurements as described here are limited in that chips must be mounted on TO-5 headers. A hot and cold stage is under development that will allow these measurements to be made in wafer form providing rapid feedback for process control.

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ERDA Contract E(49-1)-3800, Mod 3 for Jan. 1 to Sept. 30, 1976 and
ERDA Task Order A021-EES for Oct. 1 to Dec. 31, 1976

16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

This annual report describes NBS activities directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from rapidly increasing demands for electricity and the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for thyristors and rectifier diodes.

The major tasks under this project are (1) to evaluate the feasibility of the photovoltaic method as a rapid, nondestructive technique for characterizing the resistivity uniformity of high-resistivity, large-diameter silicon wafers and (2) to evaluate the use of thermally stimulated current and capacitance measurements as a means for characterizing lifetime controlling or leakage source defects in power device grade silicon wafers.

17. KEY WORDS (six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)
D-c transmission; energy conservation; measurement methods; photovoltaic method; power-device grade silicon; resistivity variations; silicon; thermally stimulated capacitance; thermally stimulated current; thermally stimulated measurements; thyristor materials measurements; thyristor measurements.

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